

System Troubleshooting
Guide

TROUBLESHOOTING

Guide

 / CYBER 960/962
Computer System

CYBER 960/962 Computer System

Troubleshooting Guide

This product is intended for use only as described in this document. Control Data cannot be responsible for the proper functioning of undescribed features and parameters.

Manual History

This manual is revision A, printed October 1988.

Revision	Change Order	Date	Reason for Change
A	-	10-07-88	Manual released.

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About This Manual

This manual trains customer engineers (CEs) to troubleshoot the CONTROL DATA® CYBER® 960 and 962 Computer Systems. After training, the CE carries this manual to a computer site that has experienced a system failure.

Normally, the CYBER Hardware Support (CHS) organization dispatches a CE to the site with specific instructions. For a CE already stationed on site, the CE must contact CHS before attempting to troubleshoot a failing system. CHS and the CE work together to resolve on-site problems.

Organization

Chapter 1 is an overview of the actions expected of a CE after arriving at the site. Chapter 2 consists of troubleshooting tables that step the CE through a logical sequence of actions. The troubleshooting tables refer to procedures and additional information in chapters 2 through 5 and the appendixes A through F. Chapter 6 contains troubleshooting information for the power distribution and warning system. Appendix G contains a glossary.

Conventions

The following conventions are used in this manual:

- When the word "press" is used in an instruction, it tells you to press the named key or keys.
For example, when you see the instruction:
Press Enter
You should press the key labeled **Enter** on your keyboard.
- When the word press precedes a string of key names that are separated by hyphens (for example **Ctrl-Alt-Del**), it means that you should press the keys listed simultaneously.
For example, when you see the instruction:
Press Ctrl-Alt-Del
You should press the keys labeled **Ctrl**, **Alt**, and **Del** simultaneously.
- When the word "type" is used in an instruction, it tells you to type in the following word.
For example, when you see the instruction:
Type TEST
You should type the letters **T E S T** in sequence.
- New features, as well as changes, deletions, and additions to this manual, are indicated by vertical bars in the margins.

Trademarks

The Zenith-248 is a product of Zenith Data Systems Corporation.

HOSTESS is a trademark of Control Systems Inc. The HOSTESS multiport network adapter is a product of Control Systems, Inc.

MS-DOS is a trademark of Microsoft Corporation.

Radio Frequency Warning

The following warning applies to all equipment described in this manual.

⚠ WARNING

This equipment generates, uses, and can radiate radio-frequency energy. If it is not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the standards set forth in the United States, Code of Federal Regulations: Title 47: Telecommunications; Chapter I - Federal Communications Commission (FCC); Part 15 - Radio Frequency (RF) Devices; Subpart J - Computing Devices which are designed to provide reasonable protection against RF interference when operated in a residential environment.

Control Data Related Manuals

The manual set figures on the next two pages show all related hardware and maintenance software manuals that are available to the CE.

CYBER 960/962 HARDWARE MANUALS

SYSTEM MANUALS

Site Preparation

General
Information
Site Preparation

60275100

Mainframe
Complex Data
Site Preparation

60000119

Peripheral
Equipment Data
Site Preparation

60275300

Installation

Mainframe
Installation and
Checkout

60000120

Operation

Virtual State
Reference

Volume 1

60000132

Virtual State
Reference

Volume 2

60000133

CYBER 170 State
Reference

60000127

19003 System
Console Operations/
Maintenance

60463610

Troubleshooting

System
Troubleshooting

60000122

Codes

System Codes
Booklet

60458100

EQUIPMENT MANUALS

Central Processing Unit (CPU)

CPU Maintenance

60000123

CPU Theory and
Diagrams

60000118

Mainframe Power and Environmental

Mainframe Power
and Environmental
Subsystem
Maintenance

60000125

Mainframe Power
and Environmental
Subsystem
Theory and
Diagrams

60000121

Input/Output Unit (IOU)

IOU Maintenance

60000130

CYBER 960 IOU Manuals

IOU Theory and
Diagrams

Levels 0-3

60463540

IOU Diagrams

Level 4

60462210

Wire Lists
Microfiche
60000134

CYBER 962 IOU Manuals

IOU Theory and
Diagrams

Levels 0-3

60000235

IOU Diagrams

Level 4

60000236

Wire Lists
Microfiche
60000135

Motor Generator (MG) Equipment

25-kVA Frequency
Converter
Hardware
Maintenance

60456520

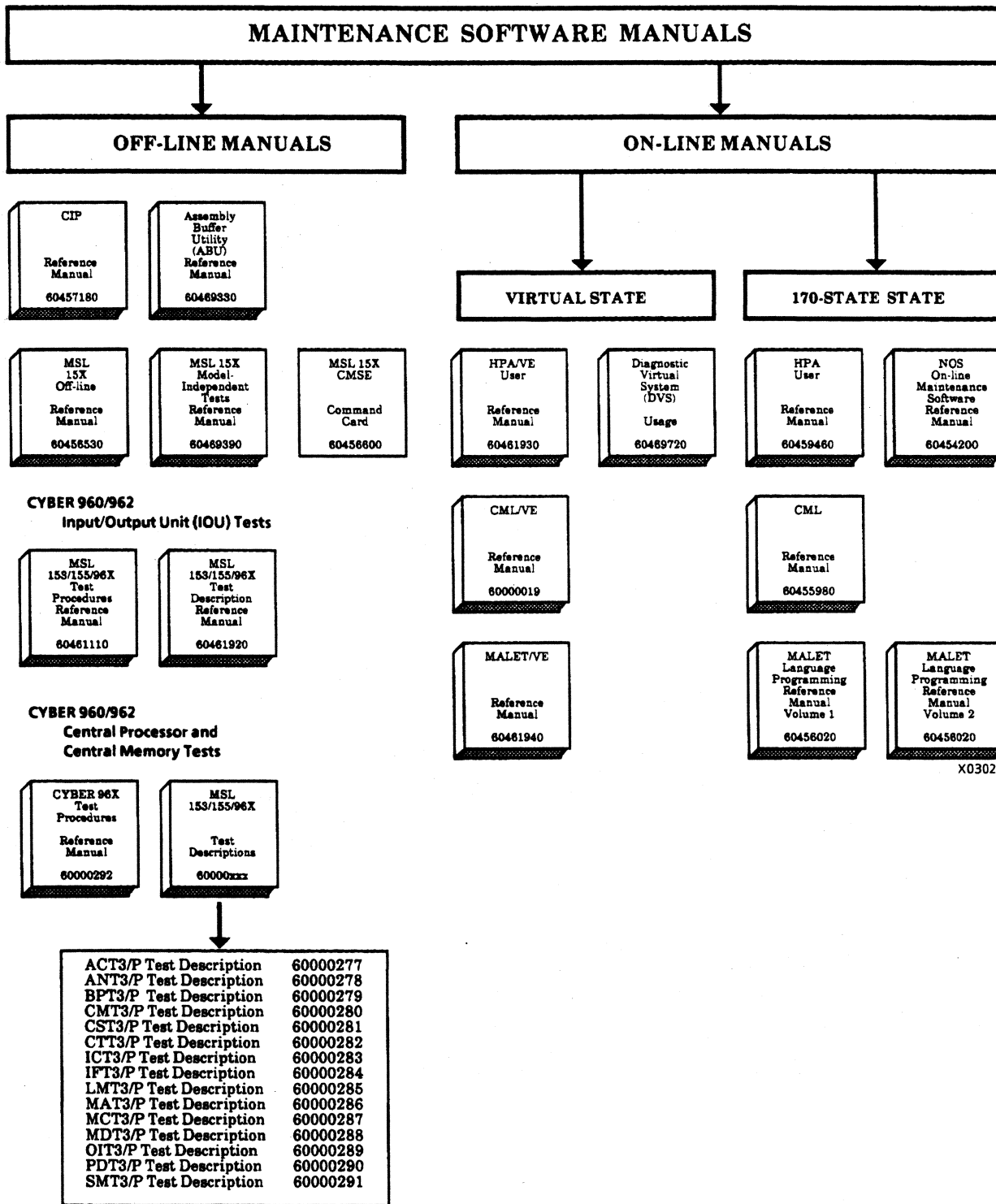
40-kVA Control
Cabinet and Motor
Generator Hardware
Maintenance

60454720

MG Interface Unit
Installation and
Maintenance

60000124

M02240



X03025

Non-Control Data Related Manuals

Other related manuals are listed below.

Title	Publication Number
Zenith Service Guide Z-200 PC Series	62950175
Zenith Z-200 Series Diagnostics and User's Guide	41621160
Zenith Z-200 PC Series Computers Owner's Manual	595-3673
Zenith High-Resolution Analog RGB Color Video Monitor User's Guide	595-3924
HOSTESS Multiport Network Adapter User's Guide	None
HOSTESS Installation Guide	None

Introduction

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Troubleshooting Overview	1-1
Removal/Replacement Overview	1-6
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This chapter provides an overview of actions a CE is expected to take when responding to a service call. Read this chapter before proceeding with any troubleshooting activities.

System Configuration

Figure 1-1 shows the full system configuration. Figures 1-2 and 1-3 show the various product configurations for the power unit, central processing unit (CPU), and input/output unit (IOU). Figure 1-4 shows the equipment configuration.

Corrective Maintenance Overview

Corrective maintenance is the systematic elimination of a fault by isolating it to a field-replaceable unit (FRU) and replacing the FRU. Recognizing a problem, locating the fault, and correcting the fault are the three steps to take when normal operation has been interrupted.

Troubleshooting Overview

When the system operator informs the CE of a problem, the CE must isolate the problem as quickly as possible. The CE must determine from the operator:

- Equipment configuration.
- Fault symptom code (FSC) displayed on system console.
- Error messages displayed on power unit and/or system console.
- If operator has done an express deadstart dump (EDD) of the operating system.

Before attempting to restart the system, the CE must go to chapter 2. The structured analysis method (SAM) tables in chapter 2 systematically step a CE through a logical sequence of troubleshooting activities.

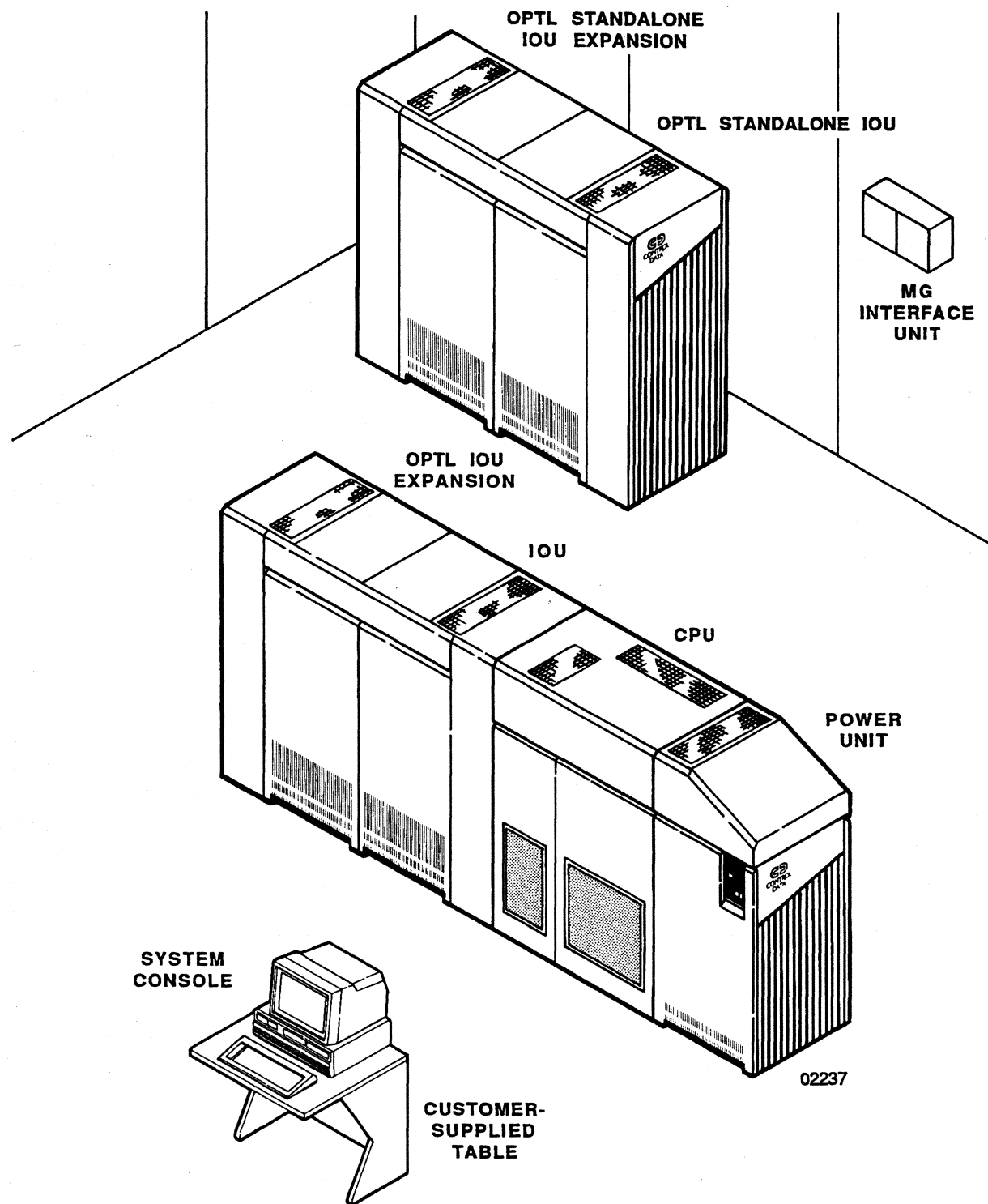


Figure 1-1. Full System Configuration

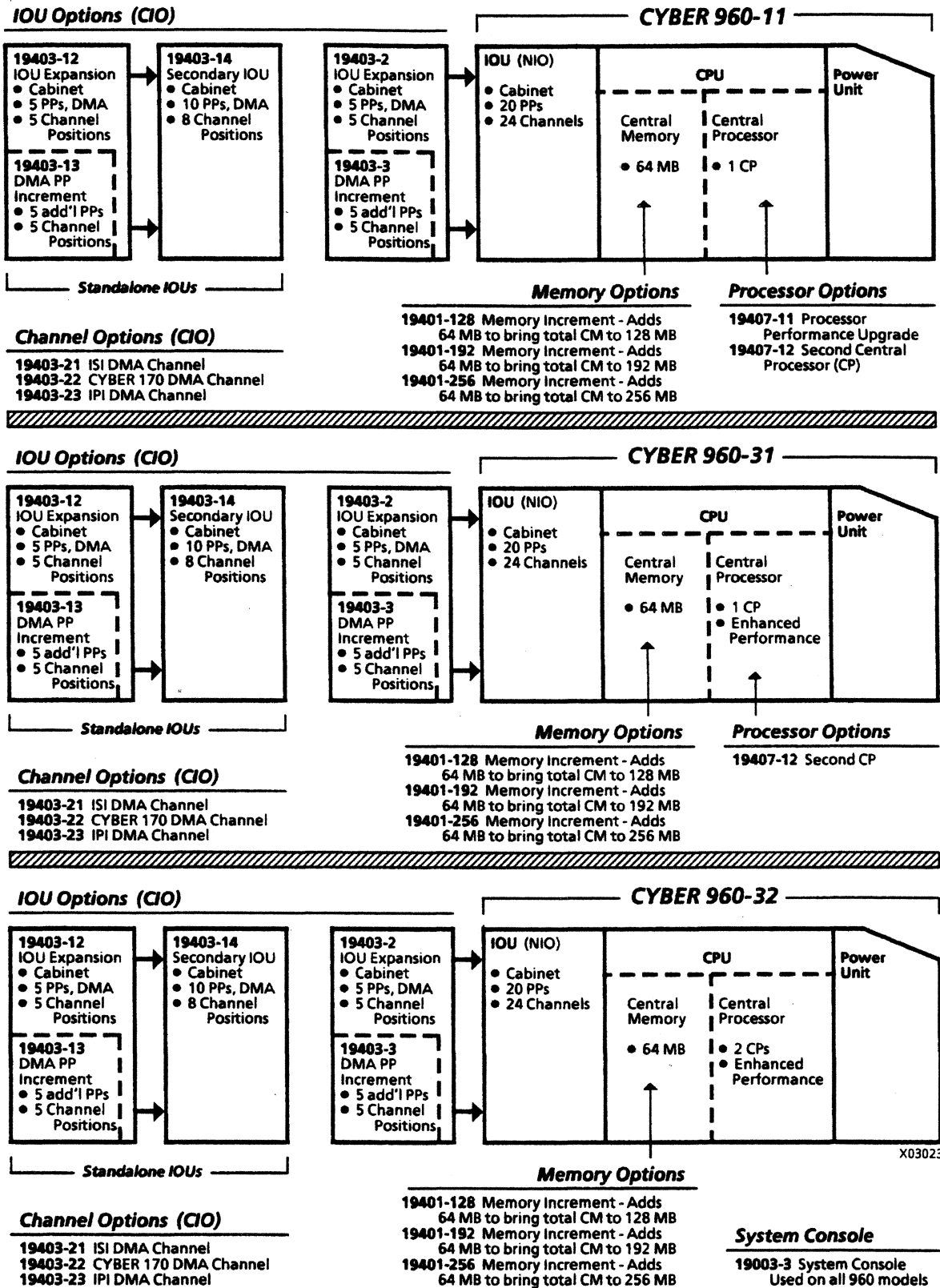


Figure 1-2. CYBER 960 Product Configuration

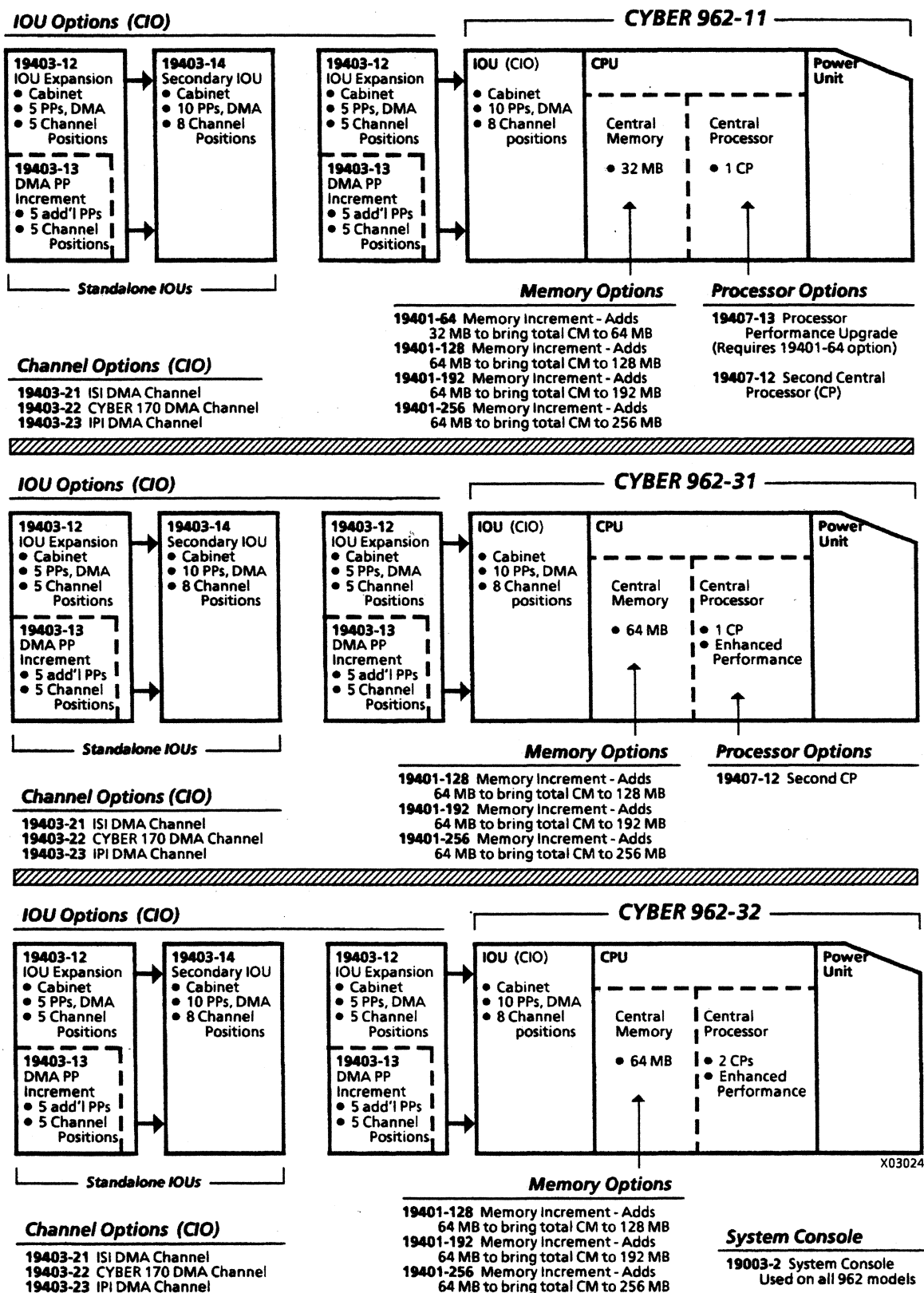
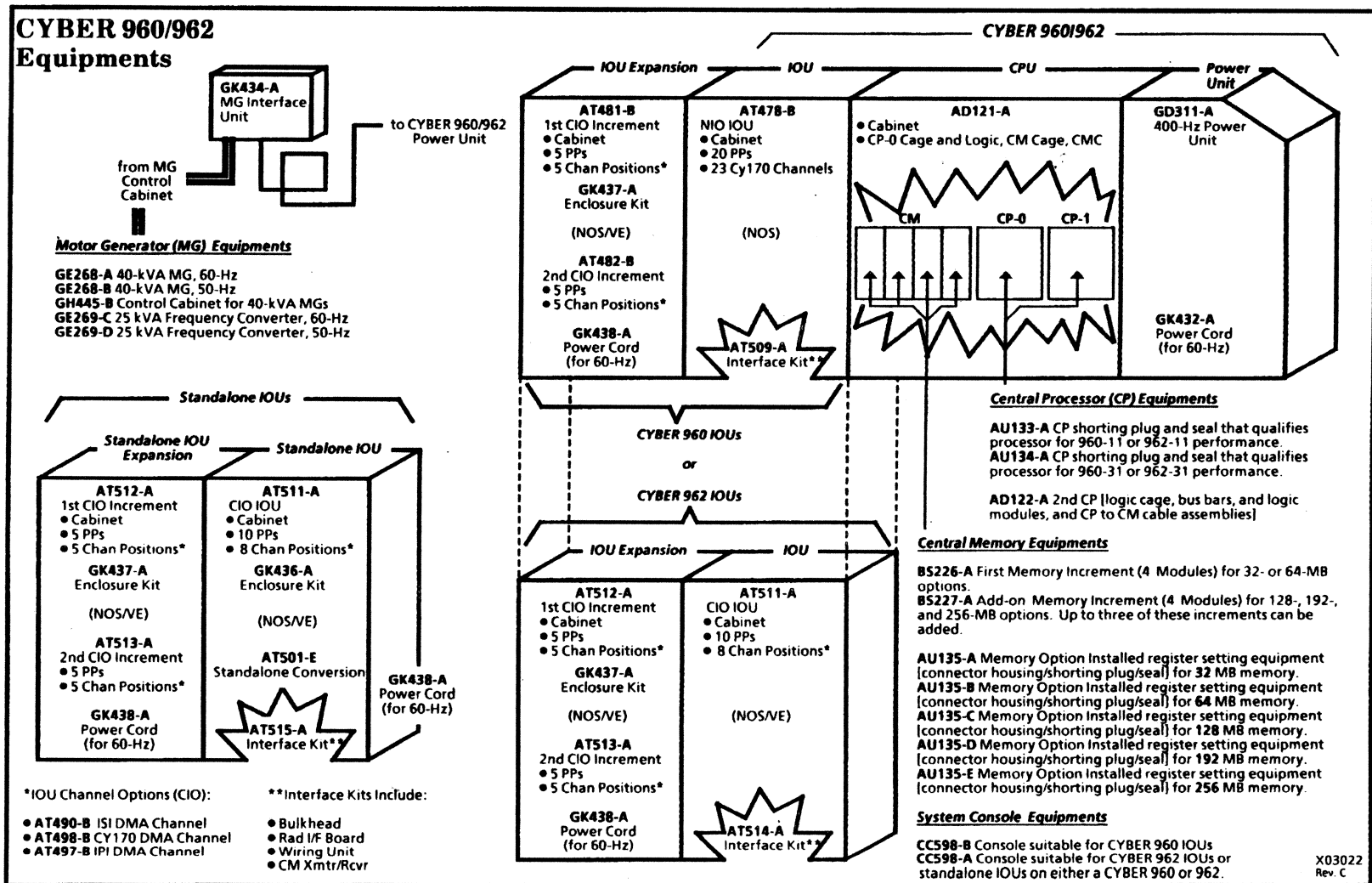


Figure 1-3. CYBER 962 Product Configuration

Figure 1-4. CYBER 960/962 Equipment Configuration



Removal/Replacement Overview

Removal/Replacement procedures are located in the hardware maintenance manuals listed in About This Manual. This is the systematic elimination of a hardware fault after the fault has been isolated to a failing FRU. Isolating the fault to a failing FRU is accomplished by using procedures in this manual or through the guidance of CHS.

After locating and correcting the fault, verify the repair using the same diagnostics that detected the fault. Unless directed otherwise, return repairable FRUs within 48 hours, and dispose of non-repairable FRUs locally.

Be sure to include the fault symptom code (FSC), if any, with the completed maintenance action form (MAF) and any special reporting forms. The FSCs, as well as solutions to corrected problems, are input to the fault symptom data base established to help others in troubleshooting and repair.

If the customer maintains a site log, be sure to make the appropriate entries in the log.

Electrostatic Discharge Requirements

To avoid damage to static-sensitive parts, follow these electrostatic discharge (ESD) requirements:

- ___ 1. Use an antistatic wrist strap, grounded to the chassis, when handling modules in the equipment.
- ___ 2. Place modules in antistatic bags when carrying them.
- ___ 3. Work only on a grounded workstation when installing field change orders (FCOs) or when handling modules away from the equipment.

For more information, refer to ES Procedure 4.500, How Electrostatic Parts are Handled.

Structured Analysis Method and Procedures

2

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Structured Analysis Method and Procedures

2

The structured analysis method (SAM) in this chapter systematically steps a CE through a logical sequence of troubleshooting activities. There are two SAM tables. SAM 2-1 (Start Troubleshooting) may direct the CE to SAM 2-2 (System Down). SAM tables direct the CE to procedures in this and other manuals.

To interpret a SAM table, go to the first step in the table. If the answer to a question is yes, follow the line below the Y to the next question or action. If the answer is no, follow the line below the N. If the first suggested action does not solve the problem, move on to the next action in the sequence. To avoid confusion, do not perform procedures out of sequence.

Assumptions:

1. Mainframe and peripheral equipment are powered up, online, and ready.
2. NORMAL/DIAGNOSTIC switch on two-port multiplexer (TPM) box is in NORMAL position (960 only).
3. TPM baud rate switch is set to 19.2K (960 only).

SAM 2-1. Start Troubleshooting (960 Only)

This SAM is the first table used when responding to a service call. The customer may have restarted the operating system since the failure. If so, start troubleshooting this intermittent failure at step 380. If this is a network operating system (NOS), start troubleshooting at step 010. If this is a NOS/virtual environment (VE), start troubleshooting at step 630.

010	Y	N				Does system console still show a NOS display (system hung)?
020		Y	N			Has customer tried to restart operating system since last failure and possibly lost status information?
030			Y	N		Has customer done an express deadstart dump (EDD) of operating system?
031				1		If Monitor display driver (MDD) is up, display dedicated fault tolerance (DFT) buffers according to procedure 2-1 in this chapter.
040				2		Initialize system console according to procedure in chapter 3.
050			Y	N		Did Console Main Menu (S, C, M) appear on screen after system console initialization?
060				Y	N	Is system console screen blank?
070					Y	Any error messages on system console screen?
080					1	Refer to system console troubleshooting procedure in chapter 3.
090					2	Call CHS or system console repair person for assistance.
100					1	Record error messages.
110					2	If problem not solved, go to step 120.
120				1		Refer to system console troubleshooting procedure in chapter 3.
130				2		Call CHS or system console repair person for assistance.
140			1			Type M and press Enter on system console.
150			Y	N		Does system have standalone IOU(s)?
	A	B	C	D	E	

	A	B	C	D	E		
160					Y	N	Did the Maintenance Options Display appear?
170						1	Check connections between system console and two-port multiplexer (TPM) in first cabinet of IOU.
180						2	Ensure hostess module is installed in system console. Run hostess diagnostics according to procedure in chapter 3. If test fails, replace hostess module and go to step 040.
190						3	Run operator's terminal interface diagnostic according to procedure in appendix C.
200					Y	N	Does diagnostic run successfully?
210						1	Replace parts in following order and run diagnostic after each replacement.
							• 1JKH module (TPM) in IOU • Hostess module in system console • RS-232-C cable that interconnects these modules.
220						<u>2</u>	Call CHS for assistance.
230						1	Replace 1JKH module in IOU.
240						<u>2</u>	Call CHS for assistance.
250					1		Record A, Q, P, and K values for each PP according to procedure 2-2 in this chapter.
260					<u>2</u>		Perform an EDD (or have customer do it) according to procedure 2-3 in this chapter. <i>It is very important to capture this information before it is lost!</i>
270				1			Go to step 160 and try a deadstart from primary IOU and then secondary (standalone) IOU.
280				<u>2</u>			Call CHS for assistance.
290			Y	N			Is system console screen blank?
300				1			If MDD is up, display DFT buffers according to procedure 2-1 in this chapter.
	A	B	C	D			

	A	B	C	D			
310				Y	N		Does system console display any error messages?
320					1		Ask customer to do a level 3 deadstart to reload operating system from central memory (CM).
330				Y	N		Did operating system reload from CM?
340					1		Ask customer to do a level 0 deadstart and enable MDD. This reloads operating system from disk and enables observation of DFT buffers in CM.
350					Y	N	Did operating system reload from disk?
351					Y	N	Did MDD come up?
351						1	Go to SAM 2-2 (System Down).
352						2	Call CHS for assistance.
353						1	Analyze error information in DFT buffers.
360						2	Go to SAM 2-2 (System Down).
370						3	Call CHS for assistance.
380					1		This was/is an intermittent problem. Let customer continue system operation.
390					2		For NOS--
							Ask customer to run maintenance jobs. Type MAINTENANCE and press Enter. If any of these jobs fail, output will go to printer. Call CHS for assistance.
							For NOS/VE--
							Ask customer to run diagnostic virtual system (DVS).
400					3		Ask customer to run hardware performance analyzer (HPA). Refer to figure 2-1 for HPA display example. Analyze any CM or maintenance register errors (IOU, CMC, CPU). Refer to appendix B for maintenance register bit descriptions.
410					4		Ask operator to do a deadstart dump interpreter (DSDI) analysis of EDD tape. Refer to figure 2-2 for DSDI output example. Analyze IOUMR, MEMMR, PROMR, and EICB registers.
	A	B	C	D	E	F	

	A	B	C	D	E	F
420						5
430						6
440					1	
450				1		
460				2		
470			1			
480			2			
490		Y	N			
500			Y	N		
510				Y	N	
520					1	
530				1		
540			1			
550			2			
560		1				
	A					

If customer had MDD up before operating system crashed, observe DFT buffers. Refer to procedure 2-1 (Displaying DFT Buffers) and figure 2-3 for DFT buffer display example.

Call CHS for assistance. If possible, have following information available.

- All information about what customer was running when system crashed.
- EDD information ready to be up-line loaded to CHS.
- A, Q, P, and K register values for all PPs.
- Maintenance register bits that are set.
- HPA information.
- Printer dumps of maintenance jobs.

This was/is an intermittent problem. Go to step 380 and treat this as a level 3 deadstart recovery from an intermittent operating system failure.

Record error message.

Go to SAM 2-2 (System Down).

If MDD was up, observe DFT buffers. Refer to procedure 2-1.

Go to step 080.

Did operating system reload and start running?

Did customer do an EDD?

Did customer have MDD up when system crashed?

Go to SAM 2-2 (System Down).

Observe DFT buffers. Refer to procedure 2-1.

Solid failure is indicated. Save EDD tape because CHS may need it if problem cannot be corrected.

Go to SAM 2-2 (System Down).

System starts to run but crashes soon after deadstart.

To present the information in this chapter in a structured format, this page has been left blank.

A				
570	Y	N		Did customer have MDD up when system crashed?
580		1		Deadstart system and bring up MDD. Refer to CIP reference manual.
590		2		Go to step 030.
600	1			Go to step 030.
610	1			Record NOS information (such as flashing messages) shown on system console.
620	2			Go to step 310.
630	Y	N		Does system console still show a NOS/VE display (system hung)?
640		1		Go to step 020.
650	1			Observe fault symptom code (FSC) in critical error window of system console.
660	2			Determine type of error.
670	Y	N		Is this a hardware error?
680		Y	N	Is this a software error?
690			1	This is an undefined error--go to step 020.
700		1		Notify customer and determine which of following actions to take.
				• Call CHS for assistance. • Run diagnostics. • Analyze DFT buffers. • Go to SAM 2-2 (System Down).
710	Y	N		Does FSC indicate failing logic module(s) in IOU, CPU, or CMC/CM?
720		1		Go to step 020.
730	1			Ask operator to deactivate NOS/VE.
740	2			Replace failing logic module(s).
750	3			Ask operator to perform level 0 deadstart.
760	4			Go to step 630.

SAM 2-2. System Down (960 Only)

This SAM is used when directed here by SAM 2-1 (Start Troubleshooting).

010	1		Initialize system console according to procedure in chapter 3.
020	Y	N	Did Control Data logo and Console Main Menu appear on screen after system console initialization?
030		1	Refer to system console troubleshooting procedure in chapter 3.
040	1		Type M and press Enter .
050	Y	N	Did Maintenance Options display appear?
060		1	Return to SAM 2-1 (Start Troubleshooting) step 160.
070	1		Type 0 or 1 and press Enter to select IOU connected to system console.
080	Y	N	Did Maintenance Options display appear?
090		1	Return to SAM 2-1 (Start Troubleshooting) step 160.
100	1		Set up a deadstart program (or have operator do it) according to procedures in appendix E.
110	2		Enable extended deadstart (EDS) by setting bit 0 of deadstart word 12.
120	3		Type L and press Enter to run long deadstart (LDS) and EDS.
130	Y	N	Did Initial Options display appear after completion of LDS and EDS?
140		1	Record A, Q, P, and K values for each PP according to procedure 2-2 in this chapter.
150		2	Perform TPM internal diagnostic (D) tests according to procedure in appendix C.
160		3	Isolate LDS/EDS error to faulty logic module according to tables in chapter 4.
170		4	Type RB 2 and press Enter to reconfigure PP barrels to place PP0 in PP20. Refer to reconfiguration procedure in appendix C, then repeat step 120.
180		5	Call CHS for assistance.
190	1		Type M to display Maintenance Options.
	A		

A		
200	2	Press Enter to display common maintenance software executive (CMSE) (CH/PP Display).
210	3	Type GO,FII40 and press Enter to run IOU tests FII40.
220	Y	N Did FII40 tests pass?
230		1 Refer to appendix A for test details.
240		2 Type AR0 to display IOU maintenance registers. Refer to appendix B for maintenance register and IOU error isolation information.
250		3 Call CHS for assistance.
260	4	Initialize system console according to procedure in chapter 3.
270	Y	N Did Control Data logo and Console Main Menu appear on screen after system console initialization?
280		1 Refer to system console troubleshooting procedure in chapter 3.
290	1	Initialize CP and CM as follows.
		• Type S or press Enter to display Initial Options. • Type U to display Utilities. • Type I to display Initial Options. • Type M to display Maintenance Options. • Press Enter to display CMSE (CH/PP Display).
300	2	Type GO,ALLMI3 and press Enter to run IOU/CP/CM model independent tests ALLMI3.
310	Y	N Did ALLMI3 tests pass?
320		1 Refer to appendix A for test details.
330		2 Type GO,ALLMD3 and press Enter to run CP/CM model dependent tests ALLMD3.
340	Y	N Did ALLMD3 tests pass?
350		1 Refer to appendix A for test details.
360		2 Type AR1 and AR2 to display CM and CP maintenance registers, respectively. Refer to appendix B for maintenance register information.
370		3 Call CHS for assistance.
380		1 Call CHS for assistance.
390	1	Ask customer to restart operating system.
400	2	Return system to customer.

MAINTENANCE ACTION LOG REPORT LIST

NOS/VE HPA/VE 02.26

REPORT 005031

ERROR INCIDENT REPORT

OPEN

PROCESSOR MODEL: CYBER 855 Class S/N: 109

PRODUCT ID: CP1_32

S/N: 209

ELEMENT NAME: CP1

REPORT GENERATED: 1988-08-23 08:24:28

 **** CPU TOTAL SUMMARIZATION REPORT ****

DATA TIME RANGE: 08:11:24 (1988-08-23) TO 08:11:24 (1988-08-23)

MESSAGE SUMMARY:	REG BIT ID	TOTAL
FAULT SYMPTOM CODE = DD32204		
UNCORRECTED ERROR, MCR BIT 0	00 32 80 00	1
DAI PE, FILE 2 CACHE READ DATA	00 32 82 21	1
DAI PE, CACHE DATA, SET 2	00 32 83 10	1
DAI MUX PE, LOCAL MEM READ DATA 3	00 32 83 12	1
WRITE DATA PARITY ERROR, BYTE 0	00 32 84 32	1
DAI WRITE DATA PE 1, BYTE 0	00 32 84 48	1

**** M1/M2/M3 errors are reported in both M1/M2/M3 and P1/P2/P3 reports ****

 DFT INTERFACE VERSION = 4 DFT PSR LEVEL =
 STATUS SUMMARY (00) = 2424 2424 2424 2424
 OPTIONS INSTALLED (12) = 0000 0000 0000 0012
 DEC (30) = 0000 0000 8FC0 0F78

08:11:33(A) (204) UNCORRECTED PROCESSOR ERROR *****
 SEQUENCE NUMBER = 0F PFS0 (80) 8000 0000 0000 0000
 1988-08-23 PFS2 (82) 0000 0400 0000 0000
 PFS3 (83) 0028 0000 0000 0000
 PFS4 (84) 0000 0000 8000 8000

CPU register 31 before halt = 0000 0000 0000 0473
 CPU register 31 after halt = 0000 0000 0000 0005
 CPU register 00 after halt = 2C2C 2C2C 2C2C 2C2C

Figure 2-1. HPA Display Example

IOUMR DISPLAY

RA = IOUMR. DUMP 04 DSDI
 0000000 CM 05.09.44. 88/05/12.(72) CY835 SN104 CDCNET DEV. NOS

RADIAL MCI =

REG	CONTENTS	DESCRIPTION
00	0000 0000 0000 0000	STATUS SUMMARY
10	0000 0000 022C C106	ELEMENT ID
12	0000 0FFF AFFF 0F07	OPTIONS INSTALLED
18	0000 0000 0000 0000	FAULT STATUS MASK
21	1803 1F0F 0000 0180	OS BOUNDS
30	0000 0000 0000 0000	DEPENDENT ENV CONTROL
40	0000 0000 0008 3F00	STATUS REG
80	0000 0000 0000 0000	FAULT STATUS 1
81	0000 0000 0000 0000	FAULT STATUS 2
A0	0000 0000 0000 0001	TEST MODE

MEMMR DISPLAY

RA = MEMMR DUMP 04 DSDI
 0000000 CM 05.09.44. 88/05/12.(72) CY835 SN104 CDCNET DEV. NOS

RADIAL MCI =

REG	CONTENTS	DESCRIPTION
00	0000 0000 0000 0000	STATUS SUMMARY
10	0000 0000 0120 0001	ELEMENT ID
12	0011 0000 0000 0000	OPTIONS INSTALLED
	BIT 11	16 MEGABYTE MEMORY
20	0100 0000 3200 0000	ENVIRON CONTROL
	BIT 34	DISABLE PORT 2
	BIT 35	DISABLE PORT 3
	BIT 38	DISABLE CORR ERR RESP
21	4000 0000 0FE0 0000	BOUNDS REG
A0	0024 5DC6 DC3A 4000	CORR ERR LOG
A4	0000 0000 0000 0000	UNCORR ERR LOG 1
A8	0000 0000 0000 0000	UNCORR ERR LOG 2

Figure 2-2. DSDI Output Example

DF DISPLAY

```

SCI/MDD - Level 96
Copyright CONTROL DATA 1988
DF
0003040219110080 DFT Control Word
000E00000042000A SECDED ID Table PTR.
001A0000004201A9 Maintenance Reg. Buffers PTR.
00370000004D0003 Model Dependent Buffer PTR.
0033007F0BF00004 NOS/VE Buffer PTR.
0000000000000000 C170 PP Resident Buffer PTR.
0011000000540001 C170 OS Buffer PTR.
0005000000490011 MR Buf. Control Words Buffer PTR.
0018000000490005 MF Element Counter Buffer PTR.
001F00000049001F DFT Control Info. Buffer PTR.
00000000004A0078 Supportive Status Buffers PTR.
003A0000004B0015 Non-Register Status Buffer PTR.
00110000004C0064 DFT Central Memory Resident PTR.
DFT = DFT VERIFIED.

```

MB DISPLAY

```

SCI/MDD - Level 96
Copyright CONTROL DATA 1988
MB
0000000000000000 Maint. Reg. Buff. Control Word
0000170705000019 Maint. Reg. Buff. Control Word
0000170806000032 Maint. Reg. Buff. Control Word
020022030100004B Maint. Reg. Buff. Control Word
0200222D02000064 Maint. Reg. Buff. Control Word
020032270340007D Maint. Reg. Buff. Control Word
0200222D04000096 Maint. Reg. Buff. Control Word
0200222D070000AF Maint. Reg. Buff. Control Word
02003227084000C8 Maint. Reg. Buff. Control Word
0200222D090000E1 Maint. Reg. Buff. Control Word
0200222D0A0000FA Maint. Reg. Buff. Control Word
020032270B400113 Maint. Reg. Buff. Control Word
0200420D0C40012C Maint. Reg. Buff. Control Word
020042190D400145 Maint. Reg. Buff. Control Word
0200422A0E4B015E Maint. Reg. Buff. Control Word
0000000000000177 Maint. Reg. Buff. Control Word
0000000000000190 Maint. Reg. Buff. Control Word

```

Figure 2-3. DFT Buffers Display Example

Procedure 2-1. Displaying Dedicated Fault Tolerance Buffers

The DF command displays the dedicated fault tolerance (DFT) control block or the contents of a DFT maintenance register buffer. If DFT has not set the verified (or rejected) flag, the message NO DFT appears on the system console screen.

NOTE

The address of the DFT control block or maintenance register buffer of interest is saved so the next memory display command also displays this portion of memory.

The format is:

DF

MB = maintenance register buffer number

The parameters are:

MB

Maintenance register buffer number to display 0 through F16. If the number is beyond the number of buffers in the mainframe, the command terminates. If the number entered is 2016, the model dependent buffer is displayed.

Procedure 2-2. Recording A, P, Q, and K Registers

Record the values in each of these PP registers as follows.

1. Type M.
2. Type PR and then press **Enter**.
3. Read the P, Q, K and A register values shown on the system console. Record this information on a copy of the deadstart record (figure 2-4) in the locations that correspond to the PP that is being checked. A range of numbers signifies that this particular PP register is in a loop. On the worksheet, note only those PPs that are hung or in a small loop.
4. Type + (to advance barrels).

DEADSTART RECORD						
PERIPHERAL PROCESSOR†	P RGTR	Q RGTR	K RGTR	A RGTR	COMMENTS††	
					PP HUNG	H 345677
					PP LOOPING	S 34567X
						L XXXXXX
N00						
N01						
N02						
N03						
N04						
N05						
N06						
N07						
N10						
N11						
N20						
N21						
N22						
N23						
N24						
N25						
N26						
N27						
N30						
N31						
C00						
C01						
C02						
C03						
C04						
C05						
C06						
C07						
C10						
C11						

† NXX is NIO PP (960) or all 962 PPs; CXX is CIO PP (960). PP numbers are all octal.
 †† Operator or CE should note whether the PP is hung (H) or looping in a large (L) or small loop (S).

M02921

Figure 2-4. Deadstart Record Worksheet

To present the information in this chapter in a structured format, this page has been left blank.

Procedure 2-3. Performing Express Deadstart Dump

Express Deadstart Dump (EDD) is an option offered on the Utilities display. It dumps the contents of PP memories, central memory, CPU hardware registers, maintenance registers, processor control store, and tape and disk (except fault symptom code) controlware to magnetic tape.

The default tape density is 800 bpi for seven-track 667/677 tapes and 1600 bpi for nine-track 639/669/679 tapes. All tapes are written in S format and as one file.

LDS and the EDS destroy parts of PP memories. If you select EDD after selecting one of these deadstart sequences, some of the information dumped is not valid. The amount of information destroyed depends on whether EDD was preceded by a short deadstart or an LDS and the setting of bit 2⁰ in word 12 (EDS) of the deadstart program.

The following locations are affected:

PP	Locations Affected During Short Deadstart Sequence	Locations Affected During LDS or LDS with EDS
PP0	0 through 52, 4275 through 77778.	All memory destroyed.
PP1 through PP4	No loss.	All memory destroyed.
All other PPs	No loss.	No loss.

NOTE

If you deadstart from a channel of an active PP, that PP loses the contents in locations 0 and 1.

If you want to dump the entire contents of PP0 memory, you must first reconfigure the PPs to deadstart from another PP or transfer the contents of PP0 memory to another PP before using EDD. Whenever possible, reconfigure the PPs. If you cannot reconfigure PPs, transfer the contents of PP0 to another PP before performing the dump. Use the following command to make the transfer:

```
MP WXX WYY (MOVE WHOLE PP MEMORY XX TO PP MEMORY YY)
```

Where: XX and YY are two-digit octal numbers.

W = N for NIO or C for CIO.

If either of the PP memories is an NIO memory in normal (4K) mode, only the lower 4K is transferred.

NOTE

If you have reconfigured PPs or moved the contents of PP0 memory, you must redeadstart to use EDD. Remember which PP received the contents of PP0 memory. Then, when the system dumps PPs, you will know which PP to print to get the contents of PP0 memory.

The following EDD procedure assumes that a dump tape has been mounted on the tape unit and the tape unit is ready. This procedure also assumes you have dead-started the system and have selected the Utilities display.

1. Type **E** to start the dump process. The console displays:

```
EXPRESS DUMP DEVICE TYPE - m
```

```
1=667, 669 ( 800 BPI)
2=667      ( 800 BPI)
   639, 679, 698 (1600 BPI)
3=639, 679, 698 (6250 BPI)
```

The value m is the device type specified in the default parameter block of the CTI/MSL disk area. If the parameter block is not present, zeros are displayed.

NOTE

If 6250 bpi is selected and the dump tape is not mounted on a 6250-bpi tape drive, the tape will be written at 1600-bpi tape density. On small tape reels, this could result in reaching end-of-tape before all data is written. This condition creates a bad dump tape. In such a case, the EDD must be restarted; however, the integrity of some of the information obtained during the second dump is questionable.

2. Press **Enter** to use the device type being displayed, or type 1, 2, or 3 and then press **Enter** to specify an alternate device. The console displays:

```
EXPRESS DUMP DEVICE TYPE - m
CHANNEL-cc
(BS) - BACK TO PREVIOUS ENTRY
```

The value cc is the channel specified in the default parameter block in the CTI/MSL disk area. If the parameter block is not present, zeros are displayed.

3. Press **Enter** to use the channel being displayed, or type the two-digit channel number of the tape unit to which data is to be dumped and press **Enter**. The console displays:

```
EXPRESS DUMP DEVICE TYPE - m
CHANNEL-cc
EQUIPMENT-e
(BS) - BACK TO PREVIOUS ENTRY
```

The value e is the equipment number specified in the default parameter block in the CTI/MSL disk area. If the default parameter block is not present, zeros are displayed.

4. Press **Enter** to use the equipment number displayed, or type the equipment number and press **Enter**. The console displays:

```
EXPRESS DUMP DEVICE TYPE - m
CHANNEL-cc
EQUIPMENT-e
UNIT-uu
(BS) - BACK TO PREVIOUS ENTRY
```

The value uu is the unit number specified in the default parameter block of the CTI/MSL disk area. If the default parameter block is not present, zeros are displayed.

5. Press **Enter** to use the unit number displayed or type the two-digit unit number and press **Enter**. The console displays:

```
EXPRESS DUMP NUMBER = 00
```

6. If the system does not have a clock chip, EDD will ask for the current day's date using the following display:

```
ENTER DATE - 00/00/00

(FORMAT YY/MM/DD)
(SPACE - SKIP FOR CHANGES)
(LEFT BLANK - ZERO ENTRY)
```

```
(BS) - BACK TO PREVIOUS ENTRY
```

7. The console displays:

```
UNLOAD DUMP TAPE OPTION

Y - UNLOAD TAPE AFTER DUMP.
N - REWIND TAPE AFTER DUMP.

(CR) - UNLOAD TAPE AFTER DUMP.
(BS) - BACK TO PREVIOUS ENTRY.
```

Type Y to have the dump tape unloaded after the dump is completed. Type N to have the tape rewound and ready when the dump is completed. The default is to have the tape unloaded.

8. For computer systems with the ECS/ESM prompt bit set in the deadstart program, the console displays:

ECS/LCM/ESM DUMP OPTIONS

(CR) = DO NOT DUMP EXTENDED
MEMORY.

NNNN = NUMBER OF 100008 WORD
BLOCKS.

(BS) - BACK TO PREVIOUS ENTRY.

Status line
Keyboard input

This display indicates how much extended memory should be dumped. Keyboard input is shown on the keyboard input line.

Type the number of 100008 word blocks of extended memory; then press **Enter** to dump extended memory or just press **Enter** to skip this option.

If a nonzero value was specified in the previous display for the number of blocks of Extended Memory to dump, and the ECS/ESM prompt bit is set in the deadstart program, the console displays:

EXTENDED MEMORY CHANNEL

(CR) = NO EM CHANNEL.

00 = CHANNEL TO DUMP EM.

(BS) = BACK TO PREVIOUS ENTRY.

This display prompts for the channel number for EDD to dump ECS/ESM.

NOTE

The ECS/ESM prompt bit (bit 2⁸ of word 13) should be set only if access to extended memory is through the low-speed port.

9. The console displays:

CONTROLWARE WILL BE DUMPED
FROM THE FOLLOWING CHANNELS

NONE (the channel numbers used are displayed here)

CONTROLWARE DUMP OPTIONS

DUMP = CH
DUMP CONTROLWARE
FROM SPECIFIED CHANNELS.

CLEAR = CH
DO NOT DUMP CONTROLWARE
FROM SPECIFIED CHANNELS.

(CR) PROCEED WITH DUMP.
(BS) - BACK TO PREVIOUS ENTRY.

Status line
Keyboard line

Channel numbers are added to this display as they are selected to be dumped.

10. Type D, then the channel number, then press **Enter** for each channel from which the controlware should be dumped. The system completes entry of the word DUMP and inserts the equal sign for you. The channel numbers are added to the list of channels to be dumped.

Type C, then the channel number, then press **Enter** to remove a channel from the list of channels to be dumped. The system completes entry of the word CLEAR and inserts an equal sign for you.

By default, no controlware will be dumped.

11. If the dump tape equipment is not ready, the console displays:

DUMP TAPE ON CHcc EQee UNuu NOT READY (CR WHEN READY)

Where: cc = channel number.
ee = equipment number.
uu = unit number.

Ready the equipment, then press **Enter** to continue.

12. If the write ring is not on the tape, the console displays:

DUMP TAPE ON CHcc EQee UNuu NO WRITE RING (CR WHEN READY)

Insert the write ring, then press **Enter**.

13. When EDD reaches the end of a tape reel before dump completion, the following message is displayed:

DUMP TAPE ON CHcc EQee UNuu WAITING REELrr (CR WHEN READY)

Where: cc = dump tape channel number.
ee = dump tape equipment number.
uu = dump tape unit number.
rr = dump tape reel number.

14. The following messages are issued when a dump tape to be written on contains label information prohibiting such action.

VSN = vvvvvv NOT ACCESSIBLE

The message indicates that the Volume Accessibility Field in the existing VOL1 label is not blank. A different tape must be used.

VSN = vvvvvv FILE NOT EXPECTED

This message indicates that the HRD1 label contains an expiration date greater than today's date, as indicated by either the calendar/clock chip or operator input. You must use an unlabeled or expired tape.

15. The existing message, EXPRESS DUMP IN PROGRESS, has been augmented by the following message:

REEL nn, VSN = vvvvvv

Where: nn is the current reel number and vvvvvv is the volume serial number of the tape being written.

16. If the tape controller does not load the character conversion tables correctly, EDD will hang and display the following message:

CHii Tj KTS CONVERSION TABLE LOAD ERRORS.
DEADSTART REQUIRED.

Where: ii = dump tape channel number.
j = 7 for seven-track dump tape.
j = 9 for nine-track dump tape.
k = M for MTS Tape Subsystem.
k = A for ATS, 67X, FSC, CCC, or 63X Tape Subsystems.

Dumping to a tape on a different channel is required.

17. Press **Enter** to initiate the dump. The following message is displayed:

EXPRESS DUMP IN PROGRESS

18. When the dump is completed, the console displays:

DUMP id COMPLETE

Where: id = dump identifier entered during sequence.

The following message is displayed if an extended memory dump was specified and extended memory could not be dumped:

DUMP id COMPLETE.
DEADSTART REQUIRED.
ECS/ESM NOT ACCESSIBLE.

On all systems, the following message is displayed if one or more of the channels selected for the controlware dump options was not able to be dumped.

DUMP id COMPLETE.
DEADSTART REQUIRED.

CONTROLWARE WAS NOT DUMPED
FROM THE FOLLOWING CHANNELS

nn	nn	nn	nn	nn	nn
nn	nn	nn	nn	nn	nn
nn	nn	nn	nn	nn	nn
nn	nn	nn	nn	nn	nn

Where: nn = the channel number to be dumped. From 1 to 24 channel numbers may be displayed.

The ECS/ESM NOT ACCESSIBLE and the CONTROLWARE WAS NOT DUMPED messages may both be displayed if the conditions that cause them to be displayed exist simultaneously.

If an error occurred during the dump, one of the following messages appears:

ERROR IN (error)
FATAL TO DUMP OPERATION

or

DUMP SUCCESSFUL
equipment
(CR) TO SEE ERROR STATUS

Error	Description
UN	Unit errors.
EQ	Controller errors.
CH	Channel errors.
Equipment	Description
BC	Buffer controller.
CM	Central memory.
ECS-LCM	Extended memory.
MMR	Memory maintenance registers.
MR	Maintenance registers.
PCS	Processor control store.
PEP	Processor exchange package.
PMR	Processor maintenance registers.
PP _i	Peripheral processors numbered consecutively ($0 \leq i \leq 17$).
PRF	Processor register file.

If you press **Enter** following this display, the system displays general and detailed equipment status information.

NOTE

If a CP is logically turned off, a flag indicating this is set in the dump, and the CP is not exchanged during EDD execution. If CP-0 is down on a single-CP system, both CP-0 and CP-1 must be logically turned off at deadstart to avoid exchanging of the registers.

If you reconfigured PPs before the dump, reconfigure them back to their normal settings after the system completes the dump.

System Console Initialization and Troubleshooting

3

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System Console Initialization and Troubleshooting

3

This chapter describes the procedures for initializing and troubleshooting the system console.

System Console Initialization

The system console can be initialized in two ways: by applying power to the console; or by pressing a combination of keys at the keyboard. The following procedures assume that you have unlocked the keyboard.

Power-On Initialization Procedure

Turn power on at the video monitor and at the console computing unit (CCU). The system console executes a series of power-on self tests. When the tests are finished, the Control Data logo appears. The system console software begins the initialization sequence and then displays the Console Main Menu (figure 3-1). PROGRAM n SELECTED (for 960) refers to one of eight two-port multiplexer (TPM) deadstart programs which can be selected. A program remains in operation until reselected.

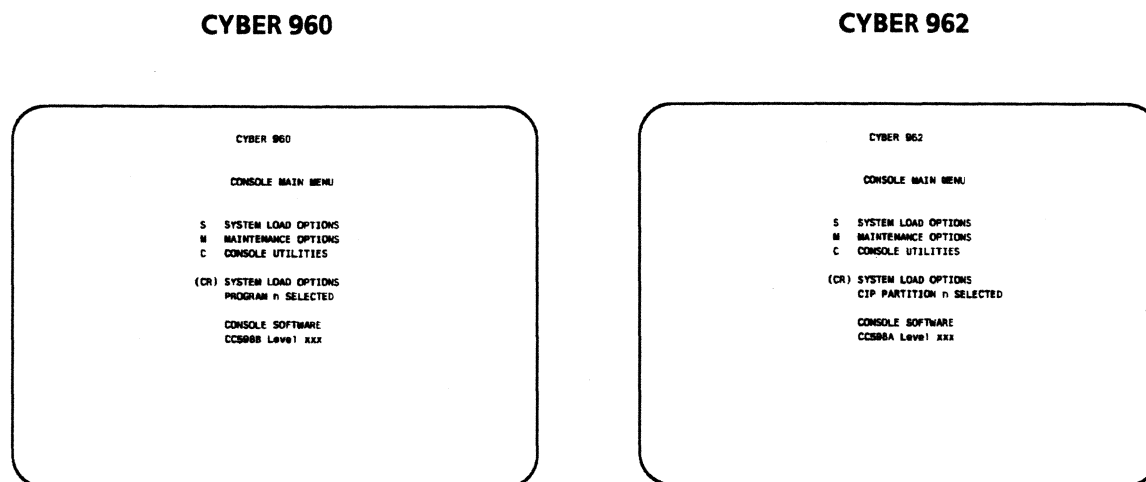


Figure 3-1. Console Main Menu Display

You may now initialize the CYBER system and load the operating system as described in the CIP Reference Manual listed in About This Manual.

If you want to reinitialize your console by turning the CCU off and then on again, wait at least five seconds before turning power on.

⚠ CAUTION

Do not power down the system console and the TPM at the same time, as the passwords may be lost.

Keyboard Initialization Sequence

To initialize the console, press **Ctrl-Alt-Del**. This can be done at any time. The system console then executes a series of self tests. When the tests are finished, the Control Data logo appears. (If the logo does not appear, you must power down the console and retry.) The system console software begins the initialization sequence and then displays the Console Main Menu (figure 3-1).

You may now initialize the CYBER system and load the operating system as described in the CIP Reference Manual.

Recovery Procedure

Should the console software fail during computer system operation, perform the following steps to resume communications with the computer system. This procedure must be executed from the system console. The computer operating system will be unaware of the console failure.

1. Press **Ctrl-F2** keys. The Console Main Menu display (figure 3-1) should appear. If this does not occur, go to step 2. If the Console Main Menu display appears, go to step 6.
2. Press **Ctrl-Alt-Del**. The system console executes a series of diagnostic self tests. When the tests are finished, the Control Data copyright should appear briefly, followed by the initialization sequence, and then by the Console Main Menu display (figure 3-1). If this does not occur, go to step 3. If the Console Main Menu display appears, go to step 6.
3. Turn system console CCU power off. Wait five seconds for the disk to stop and then turn CCU power on. The system console executes a series of power-on self tests. When the tests are finished, the Control Data copyright should appear briefly, followed by the initialization sequence, and then by the Console Main Menu display (figure 3-1). If this does not occur, go to step 4. If the Console Main Menu display appears, go to step 6.

4. Execute the Manual Diagnostics.

- a. Press
- Ctrl-Alt-Ins**
- . The console will display:

```
MFM-200 Monitor, Version x.x  
Memory Size: 640K bytes  
Enter ? for help.  
->
```

- b. Type
- TEST**
- and press
- Enter**
- . The console will display:

CHOOSE ONE OF THE FOLLOWING

```
1.DISK READ TEST  
2.KEYBOARD TEST  
3.BASE MEMORY TEST  
4.EXPANSION MEMORY TEST  
5.POWER-UP TEST  
6.EXIT
```

ENTER YOUR CHOICE:

- c. Refer to the Z-200 PC Series Computers Owner's Manual listed in About This Manual for detailed instructions for selecting and running these tests.
 - d. If a hardware error is reported, record the error indication or message and contact CHS.
5. If no hardware error was reported in step 4, refer to System Console Troubleshooting in this chapter. If the Console Main Menu display does not appear at the end of the initialization process, record the steps taken along with any error messages and indications, and contact CHS. If the Console Main Menu display appears, go to step 6.
6. When the Console Main Menu display appears, press **Ctrl-F5**.

Initializing the Hard Disk and Installing the Software

The system console is shipped ready for use. The console hard disks have been initialized and the software has been installed. In the event the hard disk has been replaced, it is necessary to initialize it prior to attempting to install any software. To make the initialization and software installation easier, the console software disk contains initialization and installation procedure files for you to use. Prior to using this procedure, however, it is first necessary to create a MS-DOS system disk and copy the files from the console software disk to this disk.

Creating an Initialization Disk

1. With power applied to the console, simultaneously press the **Ctrl-Alt-Ins** keys. The console will display:

```
MFM-200 Monitor, Version x.x
Memory Size: 640K Bytes
Enter ? for help
->
```

2. Insert the disk labeled MS-DOS Disk 1 into the floppy drive (label up) and latch the door (latch down).
3. Type **BF** and press **Enter**. The console prompts you for the date and time. If you choose, you can enter the correct date and time as shown or press **Enter** to bypass these entries.
4. After requesting the date and time, the console displays a Setup menu and asks the question:

```
Proceed with SETUP (Y/N) ?
```

5. Type **N**. The console displays the prompt for drive A:

```
A>
```

6. Type **FORMAT A:/S** and press **Enter**. The console displays the following:

```
Format Version x.xx
Copyright (C) 198x, Zenith Data Systems Corporation
```

```
Insert new disk in drive A:
and press Return when ready
```

7. Remove the MS-DOS disk 1 from the floppy disk drive and insert a blank diskette rated for double-sided, high-density use into the drive and latch the door.

8. Press **Enter**. The format operation will take a few minutes and then displays the following:

```
Format complete
System transferred
```

```
xxxxxxx bytes total disk space
xxxxxx bytes used by the system
xxxxxxx bytes available on disk
```

```
Do you want to format another disk (Y/N) ?
```

9. Type **N** and press **Enter**. The MS-DOS prompt for drive **A** is displayed.

```
A>
```

10. Remove the newly formatted disk from the floppy disk drive and insert the disk labeled MS-DOS Disk 1 into the drive and latch the door.
11. For the following steps, you will be copying files from the MS-DOS disks and the Console Software disk to the newly formatted disk. Since there is only one flexible disk drive in the console, it will be necessary to switch disks during the operation. You will be told when to switch the disks.

NOTE

Always remember that Disk A refers to the appropriate MS-DOS or Console Software disk and Disk B refers to the newly formatted disk.

12. Type **COPY A:FORMAT.COM B:** and press **Enter**. When told to Place disk B in drive A:, remove the MS-DOS disk from the disk drive and insert the newly formatted disk in its place. Press **Enter** when ready. When the message 1 File(s) copied is displayed, proceed to the next step.
13. Type **COPY A:DSKSETUP.COM B:** and press **Enter**. When told to Place disk A in Drive A:, remove the newly formatted disk from the disk drive and insert the MS-DOS Disk 1 in its place. Press **Enter** when ready. When told to Place disk B in Drive A:, remove the MS-DOS disk from the disk drive and insert the newly formatted disk in its place. Press **Enter** when ready. When the message 1 File(s) copied is displayed, proceed to the next step.
14. Type **COPY A:PART.EXE B:** and press **Enter**. When told to Place disk A in Drive A:, remove the newly formatted disk from the disk drive and insert the MS-DOS Disk 2 in its place. Press **Enter** when ready. When told to Place disk B in Drive A:, remove the MS-DOS disk from the disk drive and insert the newly formatted disk in its place. Press **Enter** when ready. When the message 1 File(s) copied is displayed, proceed to the next step.
15. Type **COPY A:ASGNPART.COM B:** and press **Enter**. When told to Place disk A in Drive A:, remove the newly formatted disk from the disk drive and insert the MS-DOS Disk 2 in its place. Press **Enter** when ready. When told to Place disk B in Drive A:, remove the MS-DOS disk from the disk drive and insert the newly formatted disk in its place. Press **Enter** when ready. When the message 1 File(s) copied is displayed, proceed to the next step.

16. Type `COPY A:PREP.EXE B:` and press **Enter**. When told to Place disk A in Drive A:, remove the newly formatted disk from the disk drive and insert the MS-DOS Disk 2 in its place. Press **Enter** when ready. When told to Place disk B in Drive A:, remove the MS-DOS disk from the disk drive and insert the newly formatted disk in its place. Press **Enter** when ready. When the message 1 File(s) copied is displayed, proceed to the next step.
17. Type `COPY A: BAT *.* B:` and press **Enter**. When told to Place disk A in Drive A:, remove the newly formatted disk from the disk drive and insert the Console Software disk in its place. Press **Enter** when ready. When told to Place disk B in Drive A:, remove the MS-DOS disk from the disk drive and insert the newly formatted disk in its place. Press **Enter** when ready. Continue switching disks when told to until the message x File(s) copied is displayed on the screen.
18. At this point, you have created a MS-DOS bootable disk for use whenever it is necessary to initialize the console's hard disk or to reinstall the MS-DOS software. This disk cannot be used to reinstall the Console Software.

Initializing the Hard Disk/Installing MS-DOS

After replacing the console's hard disk, it is necessary for you to initialize the disk and install the MS-DOS system to it prior to installing the Console Software.

1. If you have created an Initialization Disk, insert this disk in the floppy disk drive. If you have not, refer to Creating an Initialization Disk.
2. With power applied to the console, press **Ctrl-Alt-Ins**. The console displays:

```
MFM-200 Monitor, Version x.x
Memory Size: 640K Bytes
Enter ? for help
->
```

3. Type **BF** and press **Enter**. After a short period of time, a full screen message appears. Follow the directions on the screen.

NOTE

1. For the CC598-A, there are two parts to this sequence, parts 1 and 2. For the CC598-B, there are three parts, parts 1, 2, and 3. You must complete all parts in the appropriate sequence before installing the Console Software.

2. If your console is a CC598-B, step 1 of part 1 of the sequence will take approximately 1.5 hours to complete. After step 1, disregard any error messages about the disk drive or controller.

Installing Console Software

1. With power applied to the console, press **Ctrl-Alt-Ins**. The console displays:

```
MFM-200 Monitor, Version x.x  
Memory Size: 640K Bytes  
Enter ? for help  
->
```

2. Insert the disk labeled MS-DOS Disk 1 into the floppy disk drive and latch the drive.
3. Type **BF** and press **Enter**. The console prompts you for the date and time. If you choose, you can enter the correct date and time as shown or simply press **Enter** to bypass these entries.
4. After requesting the date and time, the console displays a Setup menu and asks the question:

```
Proceed with SETUP (Y/N) ?
```

5. Type **N**. The console displays the prompt for drive A:

```
A>
```

6. Remove the MS-DOS disk from the floppy disk drive and insert the Console Software disk in its place.
7. Type **INSTALL** and press **Enter**. When the CDC Logo appears on the screen, the installation is complete. Remove the Console Software disk from the floppy disk drive.

NOTE

If an IOU is not attached to the console, an error message is displayed. This is normal.

System Console Troubleshooting

These procedures help you perform problem analysis and troubleshooting for the system console and the attached multiport network adapter. You should familiarize yourself with the following diagnostics as you may be directed to run them while troubleshooting the system console:

- Z-200 power-on diagnostics
- Z-200 MFM diagnostics
- Console initialization diagnostics
- Z-200 series diagnostics
- HOSTESS multiport network adapter diagnostics

System Console Failure

A console problem is indicated when nothing happens when power is applied to the system console, there is a blank video display, and when error messages appear instead of the Control Data logo on the video display.

Use the following troubleshooting table 3-1 as a checklist to identify the possible causes of system console problems.

Table 3-1. System Console Troubleshooting

Symptom	Possible Cause
Nothing happens at power on; the green light on the front panel does not light.	• Power cord not plugged in. • Power not on at wall outlet. Check with a different appliance. • Power switch on CCU not on. • Cable that attaches light and speaker not attached to CPU module in CCU.
No video (blank display) on the monitor.	• Monitor not plugged in or turned on. • Monitor not properly connected to CCU. • Brightness control turned down. • Failure of CPU module in CCU. Refer to Zenith Service Guide. • Software not installed correctly. Refer to Installing Console Software procedure in this chapter.
Insufficient brightness.	• Brightness control turned down.
Console will not boot automatically.	• Check setup menu (figure 3-2) to ensure that hard disk drive 0 is selected as boot drive. • Refer to Zenith Service Guide. • Refer to Troubleshooting the 962 System Console procedure in this chapter (962 only).
System reset to power-on point or disk keeps rebooting.	• Loose power cord.
962 only – The console powers on but does not display the CDC logo. The screen is blank, except for a cursor in the upper left corner of the screen.	• SCSI board in slot 4 is defective and should be replaced.
960 only – The message Disk Controller is Bad is displayed on the screen at power up.	• The hard disk has not been properly initialized. Refer to Initializing the Hard Disk/Installing MS-DOS procedure in this chapter.
	Perform parts 1 and 2 of the procedure.

(Continued)

Table 3-1. System Console Troubleshooting (Continued)

Symptom	Possible Cause
962 only - The CDC logo and menu displays come up but an error is displayed whenever attempts are made to communicate with the IOU.	• Run the SCSI adapter test, SAT4. If it does not run, the problem is in the IOU. • The SCSI board in slot 3 is bad. • The SCSI differential board located under the hard disk is bad. • The cables between the console and the IOU are bad.
960 only - The message Not a bootable partition appears on the screen at power up.	• The hard disk is not initialized properly. Refer to Initializing the Hard Disk and Installing the Software in procedures in this chapter. Reinstall the software only. Perform part 2 only. Do not perform part 1. Reinstall the console software on display monitor.

System Hardware Setup/Configuration Program

Time: 10:29:28 Date: 07/19/1988 <table style="width: 100%; border-collapse: collapse;"> <tr> <th></th><th>BASE</th><th>EXTENDED</th><th>EMS</th></tr> <tr> <td>Main RAM:</td><td>640K</td><td>OK</td><td>256K</td></tr> <tr> <td>Add-On RAM:</td><td>OK</td><td>OK</td><td>---</td></tr> <tr> <td>Total:</td><td>640K</td><td>OK</td><td>---</td></tr> </table> Floppy Drive 0: 5-1/4" 1.2M Floppy Drive 1: 5-1/4" 360K Boot Drive: Floppy then Hard Disk Serial Port 1 (COM1): Enable Serial Port 2 (COM2): Enable Video Display: Enhanced Graphics Video Refresh Rate: 50 Hz 60 Hz		BASE	EXTENDED	EMS	Main RAM:	640K	OK	256K	Add-On RAM:	OK	OK	---	Total:	640K	OK	---	Operating Speed: Slow Fast Smart Hard Disk Drive 0: -Not Present- Media Type: N/A <table style="width: 100%; border-collapse: collapse;"> <tr> <td>Cylinders:</td><td>Heads:</td></tr> <tr> <td>Shp Zone:</td><td>Sectors:</td></tr> <tr> <td>Precomp:</td><td>Capacity:</td></tr> </table> Hard Disk Drive 1: -Not Present- Media Type: N/A <table style="width: 100%; border-collapse: collapse;"> <tr> <td>Cylinders:</td><td>Heads:</td></tr> <tr> <td>Shp Zone:</td><td>Sectors:</td></tr> <tr> <td>Precomp:</td><td>Capacity:</td></tr> </table>	Cylinders:	Heads:	Shp Zone:	Sectors:	Precomp:	Capacity:	Cylinders:	Heads:	Shp Zone:	Sectors:	Precomp:	Capacity:
	BASE	EXTENDED	EMS																										
Main RAM:	640K	OK	256K																										
Add-On RAM:	OK	OK	---																										
Total:	640K	OK	---																										
Cylinders:	Heads:																												
Shp Zone:	Sectors:																												
Precomp:	Capacity:																												
Cylinders:	Heads:																												
Shp Zone:	Sectors:																												
Precomp:	Capacity:																												

Enter Current Time As HH:MM:SS In 24 Hour Format
 — Use Space/Backspace to select values, Arrows to move, Esc when done —

Figure 3-2. Sample Setup Menu

Troubleshooting the 962 System Console

If you are unable to boot up the console, perform the following procedure to isolate the failing component.

1. Simultaneously press the **Ctrl-Alt-Ins** keys. The console will display the following:

```
MFM-200 Monitor, Version x.x
Memory Size: 640K Bytes
Enter ? for help
->
```

2. During the boot process and prior to seeing the above display, the following messages must appear on the screen.

```
Rancho Technology RT10-AT SCSI Host Adapter
Quick-BIOS(TM) Version xx.xx
Copyright (C) 1987 Quicksilver Software Inc.
```

```
Configuration Information:
RAM Segment: 004B
Code: C800
Base Port: 0340
DMA Channel: 05
```

```
SCSI drive installed as C:
Target ID: 00
Heads: 07H
Sectors/Trk: 1AH
Cylinders: 03D6H
```

If the above message does not appear at all:

- Check the cables between the hard disk drive and the SE SCSI board in slot 4.
- Check the jumper switches on the SE SCSI board in slot 4.
- Replace the SE SCSI board in slot 4.
- Remove the SCSI board in slot 4. With the board removed from the console, repeat step 1. The messages should not appear and the Monitor Display (as shown in step 1) should appear. If this does not occur, the Zenith CPU is at fault.

If the last section of the message does not appear or if a message appears that says there were no SCSI devices found:

- Repeat step 1.
- Check the jumper switches on the SE SCSI board in slot 4.
- Replace the SE SCSI board in slot 4.

3. If step 2 is successful, type **SETUP** and press **Enter**. The Z-200 Hardware Setup/Configuration display will appear. This display contains information vital to the console boot process. The items of interest are the **BOOT DRIVE** and the **HARD DISK DRIVE 0**. The other information is not essential.

BOOT DRIVE: Floppy then Hard Disk

HARD DISK DRIVE 0: -NOT PRESENT-

Make sure that these two entries are as shown above. If they are not, follow the directions at the bottom of the display and change them. Make sure that you save the changes as directed.

4. If steps 2 and 3 are correct, insert the MS-DOS Disk I into the flexible disk drive and repeat step 1.
When the monitor display (as shown in step 1) appears, type **BF** and press **Enter**.
If the console prompts you for the date and time, the problem is with the hard disk drive (go to step 5). If you do not get a prompt for the date and time, the problem is the Z-200 CPU.
5. If the problem is with the hard disk drive, there are several things that you can attempt prior to replacing the drive.
 - Perform the procedure under Initializing the Hard Disk/Installing MS-DOS in this chapter.
 - If the above procedure is successful (no error messages), perform the procedure under Installing Console Software in this chapter.
 - If the above procedure is unsuccessful, the disk drive must be replaced. After replacing the drive repeat this procedure.

Error Messages

The system console monitor displays an error message if the console detects a fault while powering up or if there is a communication error with the mainframe. Occasionally, other error messages may appear during operation. The display will exhibit an error code and a self-explanatory error message.

The system console performs a series of self-tests when turned on. If the console fails a test, it displays an error message instead of the Control Data logo. If the system console displays an error message at this time, refer to the System Troubleshooting chapter of the Zenith Service Guide listed in About This Manual for assistance in identifying and correcting the problem.

Console Information Lost Notification

The message on the display in figure 3-3 indicates that the TPM has been powered down and the console has lost information as follows.

- Remote Access Password
- Console Password
- Telephone List
- Communication Parameters for the Modem

Press the **space bar** to set the default values. Then reset the information to the desired settings as soon as possible.

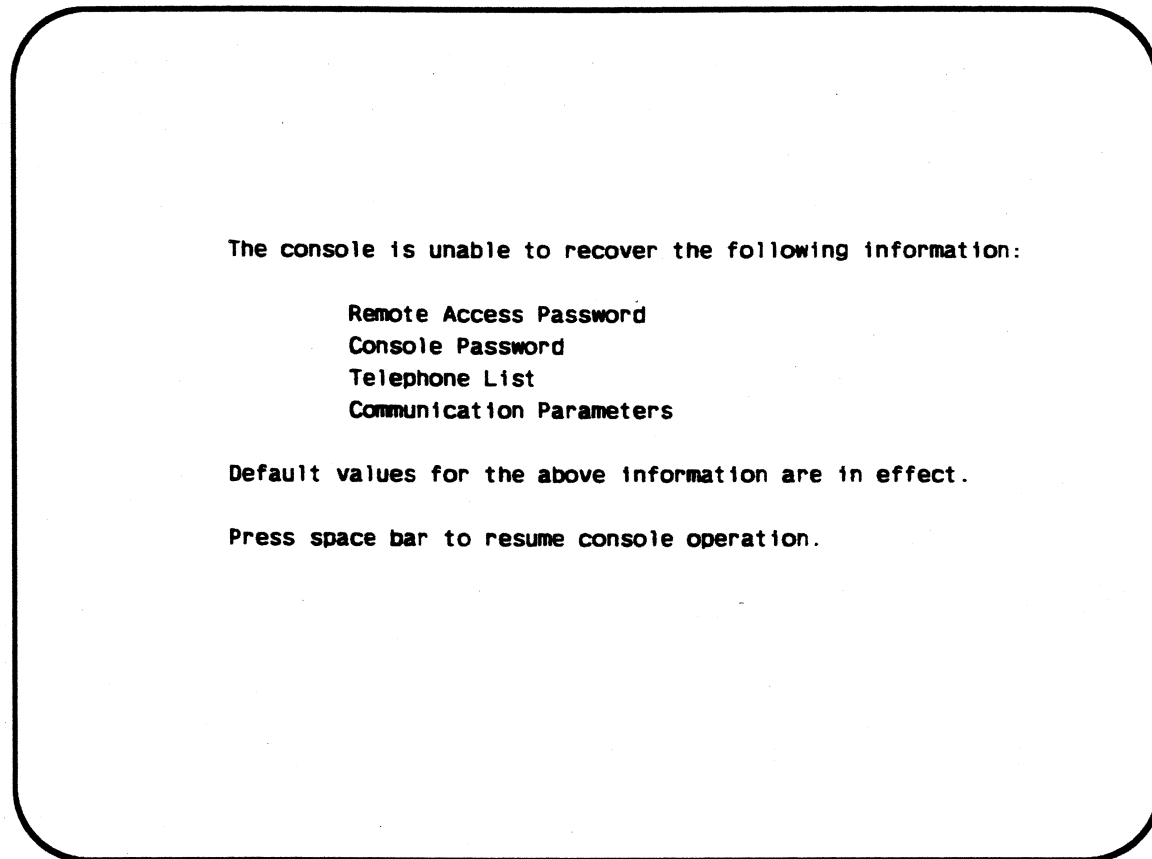


Figure 3-3. Console Information Lost Notification

Undefined Deadstart Programs in TPM

The Maintenance Options - IOU0 in the TPM Display will appear instead of the Console Main Menu display when the selected deadstart program has not been previously saved. The following message will appear at the bottom of the display:

RE-ENTER DS PROGRAMS

This occurs when a new TPM module has been installed in the mainframe.

NOTE

To bring up CMSE in the secondary IOU-1,

Type M
Type 1
Type S or L

The appropriate deadstart program must be selected in IOU-1 PP memory.

Running Multiport Network Adapter Diagnostics

Use the following procedure to test the multiport network adapter.

NOTE

This diagnostic requires you to install a test plug provided with the HOSTEST diagnostics on each of the multiport connectors. Therefore, before running the diagnostic, you must disconnect any cables connected to the multiport adapter housing. Be sure to label the cables before disconnecting them. Reconnect the cables after running the diagnostic.

1. Turn on the console.
2. Press **Ctrl-Alt-Ins** keys. The console will display:

MFM-200 Monitor, Version x.x
Memory Size: xxxK bytes
Enter ? for help.
->
3. Insert the disk labeled Bootable HOSTEST Diagnostic into the floppy disk drive. If you do not have a Bootable HOSTEST Diagnostic diskette, you should create one using the procedure provided in part 2, chapter 1 of the System Console Operations/Maintenance Guide. If you do not want to create a bootable HOSTEST diskette at this time, insert the MS-DOS Disk 1 into the floppy disk drive.
4. Latch the disk drive.
5. Type **BF** and press **Enter**. The console prompts for the date.
6. Press **Enter**. The console prompts for the time.
7. Press **Enter**. The console will display a Setup menu and ask the question:

Proceed with SETUP (Y/N)?
8. Type **N**. The monitor will display the prompt for drive A:

A>
9. If you are not using a bootable HOSTEST diagnostic diskette, remove the MS-DOS diskette from the disk drive, and insert the HOSTEST diagnostic diskette in the floppy disk drive. If you are using a bootable HOSTEST diagnostic diskette, omit this step.
10. Type **HOSTEST** and press **Enter**.
11. Enter the following information as prompted by the HOSTEST.

HOSTESS board base address: Enter 140
Number of Ports: Enter 8
System Clock Speed: Select 2 (8 MHz - 20 MHz)

12. As the HOSTEST diagnostic runs, it will direct you to install the test plug that is included in the multiport adapter package. Install the test plug on each port as you are prompted.

NOTE

For additional information and explanations of any error messages displayed, refer to the HOSTESS Multiport Network Adapter User's Guide.

13. Remove the HOSTEST diagnostic diskette.
14. Reinitialize the system console by pressing **Ctrl-Alt-Del** keys or by turning the CCU power off, waiting five seconds, and turning power on.

LDS/EDS Error Isolation Tables (960 Only)

4

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Long Deadstart Sequence

The long deadstart sequence (LDS) is a quicklook program that resides in ROMs attached to upper core of logical PP00 memory (6000 through 77778). It is possible to select any physical PP as logical PP00 by entering the RB x and RP xx commands from the keyboard. Initiating LDS sets the following conditions:

- A master clear is issued to all PPs and all error status bits cleared.
- PP00 is forced to read the test program stored in ROM.
- PP00 address is forced to 60008.
- A PP register display is brought up on the right-hand side of screen.

While LDS is executing, certain error status bits are monitored to determine if a hardware failure has been detected. If so, a message is displayed below the PP register. If LDS does not detect a hardware failure, an extended deadstart sequence (EDS) is loaded and executed.

Each error stop is indicated by a unique P register address. The CE determines what error condition was detected by examining the P register display and referring to the following LDS error tables.

When execution of LDS is finished, the short deadstart sequence is initiated using the program currently displayed on the screen.

LDS Tests

LDS performs the following sequence of tests:

1. Arithmetic Unit Test
2. PP00 Memory Test (up to location 57778)
3. One Word Channel Test
4. Block Transfer I/O Test
5. Block Transfer with Conversion Test
6. PP01 Through PP04 Memory Test
7. Multi PP Arithmetic Unit Test
8. LDS Bit Test

The following paragraphs briefly describe these tests.

Arithmetic Unit Test

The tests performed by the arithmetic unit test are:

Test	Description
Unconditional Jump Test	Checks execution of the 03 instruction and the lower 6 bits of the d portion of the instruction. Error stops are: • P stops on 0300 or 0377 instruction for single Q bit failure. • Hardware timeout counter error indicates that a multiple Q-bit failure occurred or P register failed.
Conditional Jump Test	Checks instructions 04 through 07 with $A = 0$, $A = 1$, and $A \leq 0$. Error stops are on 03 through 07 instructions.
1x Instructions Test	Checks instructions 10 through 17 using lower 6 bits of A register. Error stops are on branch instructions.
2x Instructions Test	Checks instructions 20 through 25, arithmetic operations in A with all 18 bits, and shift network. Error stops are on branch instructions.
3x Instructions Test	Checks instructions 30 through 37 using lower addresses of PP00 memory for store instructions. Error stops are on branch instructions.
4x Instructions Test	Checks instructions 40 through 47 and all 16 bits of Q register. Lower addresses of PP00 memory is used to check restore capability. Error stops are on branch instructions.
5x Instructions Test	Checks instructions 50 through 57 with and without Q flag set. Error stops are on branch instructions.
13x Instructions Test	Checks execution of instructions 130 through 137 with 16-bit operands. Error stops on branch instructions.
14x Instructions Test	Checks execution of instructions 140 through 147 with 16-bit operands. Error stops are on branch instructions.
15x Instructions Test	Checks execution of instructions 150 through 157 with 16-bit operands, with and without Q flag set. Error stops are on branch instructions.
RJM and LJM Instructions	Check execution of instructions. Test 01 and 02 using previously written addresses in lower core of PP00 memory. Error stops are on branch instructions.

PP00 Memory Test

This test executes from low addresses of PP00 memory. The test is transferred from ROMs to PP memory and checked for correct transfer. Error stop is on a branch instruction.

The test then checks PP00 memory with 10 fixed data patterns and addresses. Error stop is on branch instruction. The contents of the A register represent the failing bits. The failing pattern and failing address are stored in low addresses of PP00 memory.

PPM00

Location	Contents
348	Failing bits
358	Failing patterns
368	Failing addresses

One Word Channel Test

This test checks channels 00 through 04 and 17 with one word input/output using all possible bit combinations and channel status during input/output. These channels are tested because they are present with any IOU configuration and are essential for successful running of CMSE. Error stops are on branch instructions and are unique for each channel status and data error.

Block I/O Transfer Test

This test checks inter PP communication over the channels using a slightly modified PP memory test. A timeout counter protects PP00 from a hung condition. Error stops are on branch instructions that are unique for each channel/PP.

Block I/O Transfer with Conversion Test

This test checks inter PP communication with 12-to-16-bit and 16-to-12-bit conversion over channels 01 through 04. Error stops are on branch instructions. A timeout feature protects PP00 from a hung condition.

PP01 Through PP04 Memory Test

This test checks PP01 through 04 memories with ten-fixed patterns and addresses. Error stops are in PP00 on branch instructions. The CE is able to find failing bits, failing patterns, and failing addresses that are stored in the following locations in PP00 memory:

PPM00

Location	Contents
----------	----------

348	Failing bits
358	Failing patterns
368	Failing addresses

Multi PP Arithmetic Unit Test

This test is the same as the Arithmetic Unit Test described previously, but runs in PP01 through PP04 simultaneously. If an error is detected, the PP in which the test is running stops and P register stop lights will be the same as for the Arithmetic Unit Test. PP00 is in a loop waiting for a message from PPx indicating the test successfully passed. The looping address is unique to each PP.

LDS Bit Test

This test checks the LDS bit in the maintenance register. If the bit is clear, PP00 stops and the P register indicates an error in the maintenance register. EDS4 loading is initiated if the LDS bit is set and EDS4 is selected.

LDS Error Tables

Tables 4-1 through 4-19 are for isolation of IOU deadstart problems. The purpose of these tables is to relate LDS error stops to suspected faulty modules.

When the IOU will not deadstart or when the LDS tests stop, start troubleshooting by using the LDS error tables. Read the PP register (A, P, Q, and K) values and find the corresponding value for the P register in the LDS error tables. For a given P, the suspected failing modules' codes are listed on the same line. These codes should be used to reference table 4-43 to find the module type and location for the value of the PP reconfiguration.

Table 4-1. I/O Hang Stops

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0012	xxxx	6400	xxxxxx	KR, KB, JW
0025	0024	0500	xxxxxx	KR, KB, JW
0026	xxxx	7300	xxxxxx	JW, KR, KB
0030	xxxx	7500	xxxxxx	JW, KR, KB
0035	xxxx	7400	xxxxxx	JW, KR, KB
0043	xxxx	7200	xxxxxx	JW, KR, KB
0046	xxxx	7000	xxxxxx	JW, KR, KB
0062	xxxx	6500	xxxxxx	JW, KR, KB

Table 4-2. Stops for Channel Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0130	0130	0300	xxxxxx	JL00, JW, KR, KB
0131	0131	0300	xxxxxx	JL00, JW, KR, KB
0132	0132	0300	xxxxxx	JL00, JW, KR, KB
0133	0133	0300	xxxxxx	JL00, JW, KR, KB
0134	0134	0300	xxxxxx	JL00, JW, KR, KB
0147	0147	0300	xxxxxx	JM, JW ¹
0150	0150	0300	xxxxxx	JL00, JW, KR
			000000	JL00, JW, KR
0151	0151	0300	xxxxxx	JL00, JW, KR
			000000	JL00, JW, KR
0152	0152	0300	xxxxxx	JL00, JW, KR
			000000	JL00, JW, KR
0153	0153	0300	xxxxxx	JL00, JW, KR
			000000	JL00, JW, KR
0154	0154	0300	xxxxxx	JL00, JW, KR
			000000	JL00, JW, KR
0167	0167	0300	xxxxxx	JM, JW ¹
			000000	JM, JW ¹

Note:

1. When you detect a channel module bus failure, pull out one channel module at a time and run LDS to find which module causes the bus failures.

To present the information in this chapter in a structured format, this page has been left blank.

Table 4-3. Stops for Block Transfer Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0171	0171	0300	000000	KB, KR, JW
			034343	JW, KR
			xxxxxxx	KB, KR, JW
0172	0172	0300	000000	KB, KR, JW
			034343	JW, KR
			xxxxxxx	KB, KR, JW
0173	0173	0300	000000	KB, KR, JW
			034343	JW, KR
			xxxxxxx	KB, KR, JW
0174	0174	0300	000000	KB, KR, JW
			034343	JW, KR
			xxxxxxx	KB, KR, JW

Table 4-4. Stops for Conversion Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0201	0201	0300	xxxxxxx	JW, KB
0202	0202	0300	xxxxxxx	JW, KB
0203	0203	0300	xxxxxxx	JW, KB
0204	0204	0300	xxxxxxx	JW, KB

Table 4-5. Stops for PP Memory Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0211	0211	0300	xxxxxxx	KB, KR, JW
0212	0212	0300	xxxxxxx	KB, KR, JW
0213	0213	0300	xxxxxxx	KB, KR, JW
0214	0214	0300	xxxxxxx	KB, KR, JW

Table 4-6. Arithmetic Unit Error Stops, Unconditional Jump Error Stops

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6000	6000	0000	010000	JW, KR, KB
6001	6001	0300	010000	JW, KR, KB
6004	6004	0300	010000	JW, KR, KB
6005	6005	0300	010000	JW, KR, KB
6010	6010	0300	010000	JW, KR, KB
6012	6012	0300	010000	JW, KR, KB
6013	6013	0300	010000	JW, KR, KB
6014	6014	0300	010000	JW, KR, KB
6015	6015	0300	010000	JW, KR, KB
6016	6016	0300	010000	JW, KR, KB
6020	6020	0300	010000	JW, KR, KB
6021	6021	0300	010000	JW, KR, KB
6022	6022	0300	010000	JW, KR, KB
6023	6023	0300	010000	JW, KR, KB
6024	6024	0300	010000	JW, KR, KB
6025	6025	0300	010000	JW, KR, KB
6026	6026	0300	010000	JW, KR, KB
6027	6027	0300	010000	JW, KR, KB
6030	6030	0300	010000	JW, KR, KB
6031	6031	0300	010000	JW, KR, KB
6033	6033	0300	010000	JW, KR, KB
6034	6034	0300	010000	JW, KR, KB
6036	6036	0300	010000	JW, KR, KB
6037	6037	0300	010000	JW, KR, KB
6041	6041	0300	010000	JW, KR, KB
6042	6042	0300	010000	JW, KR, KB
6043	6043	0300	010000	JW, KR, KB
6045	6045	0300	010000	JW, KR, KB
6046	6046	0300	010000	JW, KR, KB
6050	6050	0300	010000	JW, KR, KB
6053	6053	0300	010000	JW, KR, KB
6054	6054	0300	010000	JW, KR, KB
6055	6055	0300	010000	JW, KR, KB
6056	6056	0300	010000	JW, KR, KB
6060	6060	0300	010000	JW, KR, KB
6061	6061	0300	010000	JW, KR, KB
6062	6062	0300	010000	JW, KR, KB
6066	6066	0300	010000	JW, KR, KB
6067	6067	0300	010000	JW, KR, KB
6071	6071	0300	010000	JW, KR, KB
6072	6072	0300	010000	JW, KR, KB
6074	6074	0300	010000	JW, KR, KB
6075	6075	0300	010000	JW, KR, KB
6077	6077	0300	010000	JW, KR, KB
6100	6100	0300	010000	JW, KR, KB
6102	6102	0300	010000	JW, KR, KB
6103	6103	0300	010000	JW, KR, KB
6105	6105	0300	010000	JW, KR, KB
6106	6106	0300	010000	JW, KR, KB
6110	6110	0300	010000	JW, KR, KB

(Continued)

Table 4-6. Arithmetic Unit Error Stops, Unconditional Jump Error Stops
(Continued)

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6111	6111	0300	010000	JW, KR, KB
6113	6113	0300	010000	JW, KR, KB
6114	6114	0300	010000	JW, KR, KB
6116	6116	0300	010000	JW, KR, KB
6117	6117	0300	010000	JW, KR, KB
6121	6121	0300	010000	JW, KR, KB
6122	6122	0300	010000	JW, KR, KB
6124	6124	0300	010000	JW, KR, KB
6125	6125	0300	010000	JW, KR, KB
6127	6127	0300	010000	JW, KR, KB
6130	6130	0300	010000	JW, KR, KB
6132	6132	0300	010000	JW, KR, KB
6133	6133	0300	010000	JW, KR, KB
6135	6135	0300	010000	JW, KR, KB
6140	6140	0300	010000	JW, KR, KB
6141	6141	0300	010000	JW, KR, KB
6143	6143	0300	010000	JW, KR, KB
6145	6145	0300	010000	JW, KR, KB
6146	6146	0300	010000	JW, KR, KB
6147	6147	0300	010000	JW, KR, KB
6150	6150	0300	010000	JW, KR, KB
6151	6151	0300	010000	JW, KR, KB
6153	6153	0300	010000	JW, KR, KB
6154	6154	0300	010000	JW, KR, KB
6155	6155	0300	010000	JW, KR, KB
6156	6156	0300	010000	JW, KR, KB
6157	6157	0300	010000	JW, KR, KB
6162	6162	0300	010000	JW, KR, KB
6163	6163	0300	010000	JW, KR, KB
6165	6165	0300	010000	JW, KR, KB
6166	6166	0300	010000	JW, KR, KB
6170	6170	0300	010000	JW, KR, KB
6171	6171	0300	010000	JW, KR, KB
6172	6172	0300	010000	JW, KR, KB
6173	6173	0300	010000	JW, KR, KB
6176	6176	0300	010000	JW, KR, KB
6177	6177	0300	010000	JW, KR, KB
6201	6201	0300	010000	JW, KR, KB

Table 4-7. Conditional Jump Error Stops

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6203	6202	1400	xxxxxxx	JW, KR, KB
6204	6203	0700	xxxxxxx	JW, KR, KB
6205	6204	0500	xxxxxxx	JW, KR, KB
6206	6206	0300	000000	JW, KR, KB
6207	6207	0300	010000	JW, KR, KB
6211	6211	0300	000000	JW, KR, KB
6214	6213	0700	000001	JW, KR, KB
6215	6214	0400	000000	JW, KR, KB
6216	6216	0300	000001	JW, KR, KB
6220	6220	0300	000001	JW, KR, KB
6222	6221	1500	xxxxxxx	JW, KR, KB
6223	6222	0600	xxxxxxx	JW, KR, KB
6224	6224	0300	777777	JW, KR, KB

Table 4-8. Error Stops for 1x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6226	6225	1600	xxxxxxx	JW, KR
6227	6226	0500	xxxxxxx	KR, JW
6230	6230	0300	000000	KR, JW
6233	6232	0400	000000	KR, JW
6235	6234	0400	000000	KR, JW
6237	6236	0400	000000	KR, JW
6241	6240	0400	000000	KR, JW
6243	6242	0400	000000	KR, JW
6245	6244	1700	xxxxxxx	JW, KR
6246	6245	0500	xxxxxxx	KR, JW
6251	6250	0500	xxxxxxx	KR, JW
6261	6260	0500	xxxxxxx	KR, JW
6271	6270	0500	xxxxxxx	KR, JW
6272	6271	1100	xxxxxxx	JW, KR
6274	6273	0500	xxxxxxx	KR, JW
6300	6277	0500	xxxxxxx	KR, JW
6302	6301	1200	xxxxxxx	KR, JW
6303	6302	0500	xxxxxxx	KR, JW
6307	6306	0500	xxxxxxx	KR, JW
6311	6310	1300	xxxxxxx	JW, KR
6312	6311	0500	xxxxxxx	KR, JW
6315	6314	0500	xxxxxxx	KR, JW
6317	6316	1000	xxxxxxx	JW, KR
6322	6321	0500	xxxxxxx	KR, JW
6327	6326	0500	xxxxxxx	KR, JW
6330	6327	2400	xxxxxxx	JW, KR
6331	6330	2500	xxxxxxx	JW, KR
6332	6331	2000	xxxxxxx	JW, KR
6334	6333	0500	xxxxxxx	KR, JW

(Continued)

Table 4-8. Error Stops for 1x Instructions (Continued)

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6337	6336	0400	000000	KR, JW
6342	6341	0400	000000	KR, JW
6345	6344	0400	000000	KR, JW
6350	6347	0400	000000	KR, JW
6353	6352	0400	000000	KR, JW
6356	6355	0400	000000	KR, JW
6361	6360	0400	000000	KR, JW
6364	6363	0400	000000	KR, JW
6367	6366	0400	000000	KR, JW
6372	6371	0400	000000	KR, JW
6375	6374	0400	000000	KR, JW
6400	6377	0400	000000	KR, JW
6403	6402	2100	xxxxxx	JW, KR
6405	6404	0500	xxxxxx	KR, JW
6406	6405	2300	xxxxxx	JW, KR
6410	6407	0600	xxxxxx	KR, JW
6412	6411	0500	xxxxxx	KR, JW
6413	6412	2200	xxxxxx	JW, KR
6417	6416	0500	xxxxxx	KR, JW
6425	6424	0500	xxxxxx	KR, JW
6433	6432	0500	xxxxxx	KR, JW
6441	6440	0500	xxxxxx	KR, JW
6447	6446	0500	xxxxxx	KR, JW
6474	6473	0500	xxxxxx	KR, JW
6506	6505	0400	xxxxxx	KR, JW
6510	6507	0500	xxxxxx	KR, JW

Table 4-9. Error Stops for 3x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6511	6510	3400	xxxxxx	JW, KR
6516	6515	3000	xxxxxx	JW, KR
6517	6516	0500	xxxxxx	KB, KR
6521	6520	0400	xxxxxx	KB, KR
6522	6521	3100	xxxxxx	JW, KR
6525	6524	0500	xxxxxx	KB, KR
6527	6526	3200	xxxxxx	JW, KR
6531	6530	0500	xxxxxx	KB, KR
6533	6532	3300	xxxxxx	JW, KR
6535	6534	0500	xxxxxx	KB, KR
6537	6536	3500	xxxxxx	JW, KR
6541	6540	0500	xxxxxx	KB, KR
6552	6551	0500	xxxxxx	KB, KR
6553	6552	3600	xxxxxx	JW, KR
6554	6553	3700	xxxxxx	JW, KR

Table 4-10. Error Stops for 4x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6563	6562	4400	xxxxxx	JW, KR
6566	6565	4000	xxxxxx	JW, KR
6570	6567	0500	xxxxxx	KR, KB
6572	6571	4100	xxxxxx	JW, KR
6573	6572	0500	xxxxxx	KR, KB
6574	6573	4200	xxxxxx	JW, KR
6576	6575	0500	xxxxxx	KR, KB
6577	6576	4300	xxxxxx	JW, KR
6601	6600	0500	xxxxxx	KR, KB
6602	6601	4600	xxxxxx	JW, KR
6606	6606	0300	xxxxxx	KR, KB
6611	6610	4700	xxxxxx	JW, KR
6614	6613	0500	xxxxxx	KR, KB
6616	6615	4500	xxxxxx	JW, KR
6624	6623	0500	xxxxxx	KR, KB

Table 4-11. Error Stops for 5x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6631	6630	5000	xxxxxx	JW, KR
6633	6632	5400	xxxxxx	JW, KR
6637	6636	0500	xxxxxx	KR, KB
6641	6640	5100	xxxxxx	JW, KR
6643	6642	0500	xxxxxx	KR, KB
6644	6643	5200	xxxxxx	JW, KR
6647	6646	0500	xxxxxx	KR, KB
6650	6647	5300	xxxxxx	JW, KR
6653	6652	0500	xxxxxx	KR, KB
6656	6656	0300	xxxxxx	JW, KR
6662	6661	5500	xxxxxx	KR, KB
6671	6670	0500	xxxxxx	KR, KB
6672	6671	5600	xxxxxx	JW, KR
6701	6700	0500	xxxxxx	KR, KB
6702	6701	5700	xxxxxx	JW, KR
6711	6710	0500	xxxxxx	KR, KB

Table 4-12. Error Stops for 13x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6720	6717	103400	xxxxxx	JW, KR
6723	6722	103000	xxxxxx	JW, KR
6726	6725	000500	xxxxxx	KB, KR
6727	6726	103100	xxxxxx	JW, KR
6732	6731	000500	xxxxxx	KB, KR
6734	6733	103200	xxxxxx	JW, KR
6735	6734	000500	xxxxxx	KB, KR
6737	6736	102200	xxxxxx	JW, KR
6741	6740	000500	xxxxxx	KB, KR
6743	6742	103300	xxxxxx	JW, KR
6744	6744	000300	xxxxxx	KB, KR
6747	6746	103600	xxxxxx	JW, KR
6755	6754	000500	xxxxxx	KB, KR
6756	6755	103700	xxxxxx	JW, KR
6763	6762	000500	xxxxxx	KB, KR
6765	6764	103500	xxxxxx	JW, KR
6773	6772	000500	xxxxxx	KB, KR

Table 4-13. Error Stops for 14x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7005	7004	104400	xxxxxx	JW, KR
7007	7006	104000	xxxxxx	JW, KR
7011	7010	000500	xxxxxx	KR, KB
7012	7011	104100	xxxxxx	JW, KR
7014	7013	000500	xxxxxx	KR, KB
7016	7015	104200	xxxxxx	JW, KR
7017	7016	000500	xxxxxx	KR, KB
7021	7020	102300	xxxxxx	JW, KR
7023	7022	000500	xxxxxx	KR, KB
7025	7024	104300	xxxxxx	JW, KR
7026	7026	000300	xxxxxx	KR, KB
7031	7030	104600	xxxxxx	JW, KR
7037	7036	000500	xxxxxx	KR, KB
7040	7037	104700	xxxxxx	JW, KR
7045	7044	000500	xxxxxx	KR, KB
7047	7046	104500	xxxxxx	JW, KR
7055	7054	000500	xxxxxx	KR, KB

Table 4-14. Error Stops for 15x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7062	7061	105000	xxxxxxx	JW, KR
7065	7064	000500	xxxxxxx	KR, KB
7067	7066	105400	xxxxxxx	JW, KR
7073	7072	000500	xxxxxxx	KR, KB
7074	7073	105100	xxxxxxx	JW, KR
7077	7076	000500	xxxxxxx	KR, KB
7101	7100	102400	xxxxxxx	JW, KR
7104	7103	000500	xxxxxxx	KR, KB
7106	7105	105200	xxxxxxx	JW, KR
7110	7107	000500	xxxxxxx	KR, KB
7112	7111	105300	xxxxxxx	JW, KR
7114	7114	000300	xxxxxxx	KR, KB
7117	7116	105600	xxxxxxx	JW, KR
7126	7125	000500	xxxxxxx	KR, KB
7127	7126	105700	xxxxxxx	JW, KR
7136	7135	000500	xxxxxxx	KR, KB
7140	7137	105500	xxxxxxx	JW, KR
7147	7146	000500	xxxxxxx	KR, KB

Table 4-15. Error Stops for 01 and 02 Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7164	7164	0300	xxxxxxx	JW, KR, KB
7362	7362	0300	xxxxxxx	JW, KR, KB
7363	7363	0300	xxxxxxx	JW, KR, KB
7402	7402	0300	xxxxxxx	JW, KR, KB

Table 4-16. Error Stops for IOU Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7475	0014	006400	xxxxxxx	JW, KR, KB
7476	7476	000300	xxxxxxx	JW, JM
7500	0014	006500	xxxxxxx	JW, KR, KB
7502	0014	006600	xxxxxxx	JW, KR, KB
7503	7503	000300	xxxxxxx	JW, JM
7505	0014	006700	xxxxxxx	JW, KR, KB
7507	0014	106400	xxxxxxx	JW, KR, KB
7510	7510	000300	xxxxxxx	JW, JM
7512	0014	106500	xxxxxxx	JW, KR, KB

Table 4-17. Error Stops for Multiple PP Arithmetic Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7671	01	106500	xxxxxx	JW, KR
7673	02	106500	xxxxxx	JW, KR
7675	03	106500	xxxxxx	JW, KR
7677	04	106500	xxxxxx	JW, KR

Table 4-18. Error Stops for Escape Bit Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7733	0000	7500	xxxxxx	JW, JL00, KR
7735	0000	7200	xxxxxx	JW, JL00, KR
7736	0000	7000	xxxxxx	JW, JL00, KR
7737	7736	0500	xxxxxx	JW, JL00, KR
7740	0000	7300	xxxxxx	JW, JL00, KR
7742	7741	0500	xxxxxx	JW, JL00, KR
7743	0000	7100	xxxxxx	JW, JL00, KR
7745	7744	0500	xxxxxx	JW, JL00, KR
7747	0000	7400	xxxxxx	JW, JL00, KR
7750	0000	7600	xxxxxx	JW, JL00, KR
7751	0000	7700	xxxxxx	JW, JL00, KR
7753	0000	6600	xxxxxx	JW, JL00, KR

Table 4-19. Error Stops for LDS Bit in MR Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7756	0017	7700	xxxxxx	JM, JW, JC, JS, JQ
7761	0017	7400	xxxxxx	JM, JW, JC, JS, JQ
7762	0017	7300	xxxxxx	JM, JW, JC, JS, JQ
7764	0017	7500	xxxxxx	JM, JW, JC, JS, JQ
7767	0017	7100	xxxxxx	JM, JW, JC, JS, JQ
7771	0017	7500	000000	JM, JW, JC, JS, JQ
7776	7775	0400	000000	JM, JW, JC, JS, JQ

Extended Deadstart Sequence

The extended deadstart sequence (EDS) is similar in structure to LDS. It checks the hardware needed by common maintenance software executive (CMSE) that was not tested by LDS. When LDS completes, the common test and initialization (CTI) package loads EDS4 into PP00 from the CTI device if bit 2⁰ of word 12 is set in the deadstart program.

Each error stop is indicated by a unique P register address. The CE determines which error condition was detected by examining the P register and referring to the EDS error tables.

EDS4 Tests

EDS4 performs the following sequence of tests:

1. Real Time Clock Test
2. Initial Maintenance Register Test
3. Channel 10 and 15 Test
4. Channel Flags Test

All tests are executed from PP00 and all error stops are on branch instructions. The following paragraphs briefly describe these tests.

Real Time Clock Test

This test checks operation of channel 148, the real time clock channel, with all possible clock readings (0 through 77778) to assure the clock is working properly.

Initial Maintenance Register Test

This test checks access to the IOU maintenance registers (MR) and the hardware features that are used in other tests under CMSE to assure that those features are operational.

Channel 10 and 15 Test

This test is performed only if these channels are installed, that is determined by reading the options installed register.

The test consists of one-word input/output test over channels 108 and/or 158 using 1008 different patterns, and a channel status test. Error stops are on branch instructions. PP10 is forced to the idle condition before the one-word channel test is started.

Channel Flags Test

This test checks channel flags for the channels that have been installed in the IOU. CMSE communication structure requires successful completion of this test.

EDS Error Tables

Tables 4-20 through 4-44 are for isolation of IOU deadstart problems. The purpose of these tables is to relate EDS error stops to suspected faulty modules.

When the IOU will not deadstart or when the EDS tests stop, start troubleshooting by using the EDS error tables. Read the PP register (A, P, Q, and K) values and find the corresponding value for the P register in the EDS error tables. For a given P, the suspected failing modules' codes are listed on the same line. These codes should be used to reference table 4-43 to find the module type and location for the value of the PP reconfiguration.

The tables may refer to one or both of the tables 4-43 and 4-44, depending on the value of P. The A register content is used to index other suspected failing modules.

Table 4-20. EDS Error Isolation Error Stops for Buffer Compare Routine

P Rgtr	Q Rgtr	K Rgtr	A Rgtr ¹	Suspected Failing Module(s)
0147	0147	0300	ABCD	JC, JQ
			ABCD	JQ
			ABCD	JS, JT, JQ
			ABCD	JS, JT, JQ
			ABCD	JC, JQ
			ABCD	JC, JQ
			ABCD	JC ²
			ABCD	JS, JT ³
			ABCD	JS, JT ⁴
			ABCD	JS, JT
0404	0404	0500	xxxxxx	JS, JT, JQ
0414	0414	0500	xxxxxx	JS, JT, JQ

Notes:

1. The A register has the following format:

A = The register number 00 being the status summary register and 11 being the test mode register. Bits 51 through 48.

B = The byte number in the register. Bits 54 through 52.

C = The NIO/CIO designator 0 = NIO and 1 = CIO. Bit 55.

D = The failing bit(s) in the byte. Bits 63 through 56.

2. Type keyboard command PM00,0000 and record the value of address 418 (the logical PP number). If the test value is 00 and 01 or is 03, the suspected module is KR for that barrel as indicated in table 4-43. If the test value is 02, the suspected module is JW for the barrel indicated in table 4-43. If the test value indicates none of the above, refer to table 4-42. Use the same channel number as the logical PP number specified in address 418, replace the suggested module.

3. Refer to parity error table 4-42.

4. Refer to A register versus module code table 4-44.

Table 4-21. EDS Error Isolation Error Stops for Write/Read Maintenance Register

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0426	0426	0300	xxxxxxx	JM, JQ
0437	0437	0300	xxxxxxx	JM, JQ
0450	0450	0300	xxxxxxx	JC, JS, JQ
0451	0451	0500	xxxxxxx	JC, JS, JQ
0463	0463	0300	xxxxxxx	JM, JQ
0474	0474	0300	xxxxxxx	JM, JQ
0505	0505	0300	xxxxxxx	JC, JS, JQ
0506	0506	0500	xxxxxxx	JC, JS, JQ

Table 4-22. EDS Error Isolation Error Stops for Real-Time Clock

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0734	0734	0300	xxxxxxx	JM,JW

Table 4-23. EDS Error Isolation Error Stops for Response on Function

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0743	0743	0300	xxxxxxx	JM, JQ
0747	0747	0300	xxxxxxx	JM, JQ
0756	0756	0300	xxxxxxx	JM, JQ
0761	0761	0300	xxxxxxx	JM, JQ
0776	0776	0300	xxxxxxx	JM, JQ
1014	1014	0300	xxxxxxx	JM, JQ
1017	1017	0300	xxxxxxx	JM, JQ
1022	1022	0300	xxxxxxx	JM, JQ
1027	1027	0300	xxxxxxx	JM, JQ
1034	1034	0300	xxxxxxx	JM, JQ

Table 4-24. EDS Error Isolation Error Stops for Maintenance Channel Timeout

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1047	1047	0300	xxxxxxx	JM, JQ
1052	1052	0300	xxxxxxx	JM, JQ
1056	1056	0300	xxxxxxx	JM, JQ
1061	1061	0300	xxxxxxx	JM, JQ
1064	1064	0300	xxxxxxx	JM, JQ
1070	1070	0300	xxxxxxx	JM, JQ
1073	1073	0300	xxxxxxx	JM, JQ
1105	1105	0300	xxxxxxx	JM, JQ

Table 4-25. EDS Error Isolation Error Stops for Echo Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1142	1142	0300	xxxxxxx	JQ, JM
1145	1145	0300	xxxxxxx	JQ, JM
1151	1151	0300	xxxxxxx	JQ, JM
1154	1154	0300	xxxxxxx	JQ, JM
1161	1161	0300	xxxxxxx	JQ, JM
1164	1164	0300	xxxxxxx	JQ, JM
1171	1171	0300	xxxxxxx	JQ, JM
1174	1174	0300	xxxxxxx	JQ, JM
1200	1200	0300	xxxxxxx	JQ, JM
1204	1204	0300	xxxxxxx	JQ, JM
1212	1212	0300	xxxxxxx	JQ, JM
1220	1220	0300	xxxxxxx	JQ, JM
1223	1223	0300	xxxxxxx	JQ, JM
1227	1227	0300	xxxxxxx	JQ, JM

Table 4-26. EDS Error Isolation Error Stops for Clear Fault Status Register 1

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1242	1242	0300	xxxxxx	JS, JQ
1245	1245	0300	xxxxxx	JS, JQ
1252	1252	0300	xxxxxx	JS, JQ
1255	1255	0300	xxxxxx	JS, JQ
1261	1261	0300	xxxxxx	JS, JQ
1264	1264	0300	xxxxxx	JS, JQ
1272	1272	0300	xxxxxx	JS, JQ
1275	1275	0300	xxxxxx	JS, JQ
1301	1301	0300	xxxxxx	JS, JQ
1305	1305	0300	xxxxxx	JS, JQ
1313	1313	0300	xxxxxx	JS, JQ
1316	1316	0300	xxxxxx	JS, JQ
1321	1321	0300	xxxxxx	JS, JQ
1333	1333	0300	xxxxxx	JS, JQ
1343	1343	0300	xxxxxx	JS, JQ
1346	1346	0300	xxxxxx	JS, JQ
1352	1352	0300	xxxxxx	JS, JQ
1355	1355	0300	xxxxxx	JS, JQ

Table 4-27. EDS Error Isolation Error Stops for Clear Fault Status Register 2

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1363	1363	0300	xxxxxx	JT, JQ
1366	1366	0300	xxxxxx	JT, JQ
1372	1372	0300	xxxxxx	JT, JQ
1376	1376	0300	xxxxxx	JT, JQ
1402	1402	0300	xxxxxx	JT, JQ
1405	1405	0300	xxxxxx	JT, JQ
1411	1411	0500	xxxxxx	JT, JQ
1414	1414	0300	xxxxxx	JT, JQ
1420	1420	0300	xxxxxx	JT, JQ
1430	1430	0300	xxxxxx	JT, JQ
1433	1433	0300	xxxxxx	JT, JQ
1437	1437	0300	xxxxxx	JT, JQ
1442	1442	0300	xxxxxx	JT, JQ
1447	1447	0300	xxxxxx	JT, JQ
1452	1452	0500	xxxxxx	JT, JQ

Table 4-28. EDS Error Isolation Error Stops for Environmental Control Register

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1457	1457	0300	xxxxxxx	JT, JQ
1462	1462	0300	xxxxxxx	JT, JQ
1467	1467	0300	xxxxxxx	JT, JQ
1472	1472	0300	xxxxxxx	JT, JQ
1476	1476	0300	xxxxxxx	JT, JQ
1501	1501	0300	xxxxxxx	JT, JQ
1505	1505	0300	xxxxxxx	JT, JQ
1511	1511	0500	xxxxxxx	JT, JQ
1515	1515	0300	xxxxxxx	JT, JQ
1520	1520	0300	xxxxxxx	JT, JQ
1524	1524	0500	xxxxxxx	JT, JQ
1527	1527	0300	xxxxxxx	JT, JQ
1533	1533	0300	xxxxxxx	JT, JQ

Table 4-29. EDS Error Isolation Error Stops for Test Mode Register

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1540	1540	0300	xxxxxxx	JS, JQ
1543	1543	0300	xxxxxxx	JS, JQ
1547	1547	0300	xxxxxxx	JS, JQ
1552	1552	0300	xxxxxxx	JS, JQ
1560	1560	0300	xxxxxxx	JS, JQ
1563	1563	0300	xxxxxxx	JS, JQ
1567	1567	0300	xxxxxxx	JS, JQ
1573	1573	0300	xxxxxxx	JS, JQ
1577	1577	0300	xxxxxxx	JS, JQ
1602	1602	0300	xxxxxxx	JS, JQ
1612	1612	0300	xxxxxxx	JS, JQ
1615	1616	0300	xxxxxxx	JS, JQ
1626	1626	0300	xxxxxxx	JS, JQ

Table 4-30. EDS Error Isolation Error Stops for Maintenance Register Selects

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1644	1644	0500	xxxxxxx	JC, JQ
1653	1653	0400	xxxxxxx	JC, JQ
1660	1660	0400	xxxxxxx	JC, JQ
1667	1667	0400	xxxxxxx	JC, JQ
1674	1674	0500	xxxxxxx	JC, JQ

Table 4-31. EDS Error Isolation Error Stops for One Byte Write All Byte Reads

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
2005	2005	0500	xxxxxx	JM,JQ ¹

Note:

1. Type keyboard command PM00,0000 and record the value of:

Address 33₈ - failing byte number.

Address 34₈ - test byte that was written.

Address 35₈ - register number that was written.

Address 36₈ - test pattern that was written.

Address 37₈ - register being read.

Table 4-32. EDS Error Isolation Error Stops for Reading A Register

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
2163	2163	0500	xxxxxx	JC, JQ, KR - Logic PP 0-4
2174	2174	0500	xxxxxx	JC, JQ, KR - Logic PP 4-11
2204	2204	0500	xxxxxx	JC, JQ, KR - Logic PP 20-25
2215	2215	0500	xxxxxx	JC, JQ, KR - Logic PP 26-31

Table 4-33. EDS Error Isolation Error Stops for Channel Flags

P Rgtr	Q Rgtr	K Rgtr	A Rgtr ¹	Suspected Failing Module(s)
2446	2446	0300	xxxxCC	JW, KB, KR
3452	3452	0300	xxxxCC	JW, KB, KR
3454	3454	0300	xxxxCC	JW, KB, KR
3456	3456	0300	xxxxCC	JW, KB, KR
3457	3457	0300	xxxxCC	JW, KB, KR

Note:

1. CC = Channel number. Refer to table 4-44.

Table 4-34. EDS Error Isolation Error Stops for Fault Status Register 1 of CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0713	0713	0300	xxxxxx	JS, JQ
0716	0716	0300	xxxxxx	JS, JQ
0723	0723	0300	xxxxxx	JS, JQ
0726	0726	0300	xxxxxx	JS, JQ
0732	0732	0300	xxxxxx	JS, JQ
0735	0735	0300	xxxxxx	JS, JQ
0743	0743	0300	xxxxxx	JS, JQ
0746	0746	0300	xxxxxx	JS, JQ
0752	0752	0300	xxxxxx	JS, JQ
0756	0756	0300	xxxxxx	JS, JQ
0764	0764	0300	xxxxxx	JS, JQ
0767	0767	0300	xxxxxx	JS, JQ
0772	0772	0300	xxxxxx	JS, JQ
1004	1004	0300	xxxxxx	JS, JQ
1014	1014	0300	xxxxxx	JS, JQ
1017	1017	0300	xxxxxx	JS, JQ
1023	1023	0300	xxxxxx	JS, JQ
1026	1026	0300	xxxxxx	JS, JQ

Table 4-35. EDS Error Isolation Error Stops for Fault Status Register 2 of CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1034	1034	0300	xxxxxx	JT, JQ
1037	1037	0300	xxxxxx	JT, JQ
1043	1043	0300	xxxxxx	JT, JQ
1047	1047	0300	xxxxxx	JT, JQ
1052	1052	0300	xxxxxx	JT, JQ
1056	1056	0300	xxxxxx	JT, JQ
1062	1062	0500	xxxxxx	JT, JQ
1065	1065	0300	xxxxxx	JT, JQ
1071	1071	0300	xxxxxx	JT, JQ
1101	1101	0300	xxxxxx	JT, JQ
1104	1104	0300	xxxxxx	JT, JQ
1110	1110	0300	xxxxxx	JT, JQ
1113	1113	0300	xxxxxx	JT, JQ
1120	1120	0300	xxxxxx	JT, JQ
1123	1123	0500	xxxxxx	JT, JQ

Table 4-36. EDS Error Isolation Error Stops for Environment Control Register of CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1130	1130	0300	xxxxxx	JT, JQ
1133	1133	0300	xxxxxx	JT, JQ
1140	1140	0300	xxxxxx	JT, JQ
1143	1143	0300	xxxxxx	JT, JQ
1147	1147	0300	xxxxxx	JT, JQ
1152	1152	0300	xxxxxx	JT, JQ
1156	1156	0300	xxxxxx	JT, JQ
1162	1162	0300	xxxxxx	JT, JQ
1166	1166	0300	xxxxxx	JT, JQ
1171	1171	0300	xxxxxx	JT, JQ
1175	1175	0500	xxxxxx	JT, JQ
1200	1200	0300	xxxxxx	JT, JQ
1204	1204	0300	xxxxxx	JT, JQ

Table 4-37. EDS Error Isolation Error Stops for Test Mode Register of CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1211	1211	0300	xxxxxx	JT, JQ
1214	1114	0300	xxxxxx	JT, JQ
1220	1120	0300	xxxxxx	JT, JQ
1223	1223	0300	xxxxxx	JT, JQ
1231	1231	0300	xxxxxx	JT, JQ
1234	1234	0300	xxxxxx	JT, JQ
1240	1240	0300	xxxxxx	JT, JQ
1244	1244	0300	xxxxxx	JT, JQ
1250	1250	0300	xxxxxx	JT, JQ
1253	1253	0300	xxxxxx	JT, JQ
1263	1263	0300	xxxxxx	JT, JQ
1266	1266	0300	xxxxxx	JT, JQ
1277	1277	0300	xxxxxx	JT, JQ

Table 4-38. EDS Error Isolation Error Stops for Maintenance Register Selects in CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1315	1315	0500	xxxxxx	JU, JQ
1324	1324	0400	xxxxxx	JU, JQ
1331	1331	0500	xxxxxx	JU, JQ

Table 4-39. EDS Error Isolation Error Stops for One Byte Write All Byte Read in CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1466	1466	0500	xxxxxxx	JM, JQ ¹

Note:

1. Type keyboard command PM00,0000 and record the value of:

Address 338 - failing byte number.

Address 348 - test byte that was written.

Address 358 - register number that was written.

Address 368 - test pattern that was written.

Address 378 - register being read.

Table 4-40. EDS Error Isolation Error Stops for Reading A Register of CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
1603	1603	0500	xxxxxxx	JU, JQ, KR
1614	1614	0500	xxxxxxx	JU, JQ, KR

Table 4-41. EDS Error Isolation Error Stops for Channel Flags for CIO

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
2103	2103	0300	xxxxxx	JW, KB, KR
2107	2107	0300	xxxxxx	JW, KB, KR

Table 4-42. Parity Error Table for A=7xxxxx

Byte	Reading In Hex	Module Code
4	8x	JW
	4x	KR
	2x	JA
	1x	KB
	x8	JC
5	8x	KB
	4x	KB
	2x	KB
	1x	KB
	x8	JW
	x4	JC
	x2	JC
	x1	JW

Module Location

Module locations (table 4-43) of JW, KR, and KB depend on barrel configuration (RB=0 through 3). All other module locations are not affected by the barrel reconfiguration.

Table 4-43. IOU Module Locations

Module Code	Module	Module Location	Comment
JW	1JWH	(Note 1)	Microcode and conversion module
KR	1KRH	(Note 2)	P, Q, K, and A registers
KB	1KBH	(Note 3)	PP memory module
JC, JU	1JCH, 1JUH	A11, A10	CM address and PP MAC control
JK	1JKH	B23	TPM Module
JS	1JSH	A20	Maintenance register A module
JT	1JTH	A21	Maintenance register B module
JQ	1JQH	A22	MAC module
JA	1JAH	A01	Master clock module
JM	1JMH	B01	Maintenance channels (15,17)
JL00	1JLH	B21	Channels 0 and 1
JL02	1JLH	B20	Channels 2 and 3
JL04	1JLH	B19	Channels 4 and 5
JL06	1JLH	B18	Channels 6 and 7
JL10	1JLH	B17	Channels 10 and 11
JL12	1JLH	B16	Channels 12 and 13
JL20	1JLH	B07	Channels 20 and 21
JL22	1JLH	B06	Channels 22 and 23
JL24	1JLH	B05	Channels 24 and 25
JL26	1JLH	B04	Channels 26 and 27
JL30	1JLH	B03	Channels 30 and 31
JL32	1JLH	B02	Channels 32 and 33
CQ00	1CQ0	B22	Display controller

Notes:

1. Module locations are B14 (RB=0), B12 (RB=1), B10 (RB=2), B08 (RB=3).
2. Module locations are B15 (RB=0), B13 (RB=1), B11 (RB=2), B09 (RB=3).
3. Module locations are B28 (RB=0), B27 (RB=1), B26 (RB=2), B25 (RB=3).

Use of A Register for Fault Isolation

In LDS and EDS, the A register display indicates the failing bit(s). Use table 4-44 to find the suspected module(s) in conjunction with LDS and EDS error tables 4-1 through 4-42.

Table 4-44. A Register Versus Module Code

A Register	Module Code¹
104001	JL00
104002	JL00
104004	JL02
104010	JL02
104020	JL04
104040	JL04
104100	JL06
104200	JL06
105001	CQ00
105002	JL10
105004	JL12
105010	JL13
105040	JM
105200	JM
106001	JL20
106002	JL20
106004	JL22
106010	JL22
106020	JL24
106040	JL24
106100	JL26
106200	JL26
107001	JL30
107002	JL30
107004	JL32
107010	JL32

Note:

1. Refer module code to table 4-43 to isolate module type and location.

LDX Error Isolation Tables (962 Only) 5

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LDX Tests	5-1
Arithmetic Unit Test	5-2
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Block I/O Transfer Test	5-3
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Multi PP Arithmetic Unit Test	5-3
LDX Bit Test	5-3
LDX Error Tables	5-4
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Long Deadstart Sequence

The long deadstart sequence (LDX) is a quicklook program that resides in ROMs attached to upper core of logical PP00 memory (5400 through 7777₈). LDX transfers to barrel 1 after barrel 0 completes. LDX continues to transfer to barrels 2 and 3 if they are installed. PPs within each barrel may be reconfigured by using the deadstart display and entering the RP X command. Initiating LDX sets the following conditions:

- A master clear is issued to all PPs and all error status bits cleared.
- PP00 is forced to read the test program stored in ROM.
- PP00 address is forced to 6000₈ (5400 through 5700₈ is for test update and transfer routine).
- A PP register display is brought up on the right-hand side of screen.

While LDX is executing, certain error status bits are monitored to determine if a hardware failure has been detected. If so, a message is displayed below the PP register.

Each error stop is indicated by a unique P register address. The CE determines what error condition was detected by examining the P register display and referring to the following LDX error tables.

When execution of LDX is finished (all installed barrels run), the short deadstart sequence is initiated using the program currently displayed on the screen.

LDX Tests

LDX performs the following sequence of tests:

Test Name

Arithmetic Unit Test
PP Memory Test (up to location 5377₈)
One Word Channel Test
Block Transfer I/O Test
Block Transfer with Conversion Test
Multi PP Arithmetic Unit Test
LDX Bit Test

The following paragraphs briefly describe these tests.

Arithmetic Unit Test

The tests performed by the arithmetic unit test are:

Test	Description
Unconditional Jump Test	Checks execution of the 03 instruction and the lower 6 bits of the d portion of the instruction. Error stops are: • PP stops on 0300 or 0377 instruction for single Q bit failure. • Hardware timeout counter error indicates that a multiple Q-bit failure occurred or P register failed.
Conditional Jump Test	Checks instructions 04 through 07 with $A = 0$, $A = 1$, and $A \leq 0$. Error stops are on 03 through 07 instructions.
1x Instructions Test	Checks instructions 10 through 17 using lower 6 bits of A register. Error stops are on branch instructions.
2x Instructions Test	Checks instructions 20 through 25, arithmetic operations in A with all 18 bits, and shift network. Error stops are on branch instructions.
3x Instructions Test	Checks instructions 30 through 37 using lower addresses of PP memory for store instructions. Error stops are on branch instructions.
4x Instructions Test	Checks instructions 40 through 47 and all 16 bits of Q register. Lower addresses of PP memory is used to check restore capability. Error stops are on branch instructions.
5x Instructions Test	Checks instructions 50 through 57 with and without Q flag set. Error stops are on branch instructions.
13x Instructions Test	Checks execution of instructions 130 through 137 with 16-bit operands. Error stops on branch instructions.
14x Instructions Test	Checks execution of instructions 140 through 147 with 16-bit operands. Error stops are on branch instructions.
15x Instructions Test	Checks execution of instructions 150 through 157 with 16-bit operands, with and without Q flag set. Error stops are on branch instructions.
RJM and LJM Instructions	Check execution of instructions. Test 01 and 02 using previously written addresses in lower core of PP memory. Error stops are on branch instructions.

PP Memory Test

This test executes from low addresses of PP memory. The test is transferred from ROMs to PP memory and checked for correct transfer. Error stop is on a branch instruction (PP00 at location 248, PP01 through PP04 at PP00 memory location 2108 plus PP number).

The test then checks PP memory with 10 fixed data patterns and addresses. Error stop is on branch instruction. The contents of the A register represent the failing bits. The failing pattern and failing address are stored in low addresses of PP00 memory.

PPM00

Location	Contents
348	Failing bits
358	Failing patterns
368	Failing addresses

One Word Channel Test

This test checks channels with one word input/output using all possible bit combinations and channel status during input/output. Barrel 0 tests channels 0, 1, and 13. All other barrels test channels 12, 15, and 17. The remaining channels are not tested because they may not be installed. Error stops are on branch instructions and are unique for each channel status and data error.

Block I/O Transfer Test

This test checks inter PP communication channel 12 using a slightly modified PP memory test. A timeout counter protects PP00 from a hung condition. Error stops are on branch instructions that are unique for each channel/PP.

Block I/O Transfer with Conversion Test

This test checks inter PP communication with 12- to 16-bit and 16- to 12-bit conversion over channel 12. Error stops are on branch instructions. A timeout feature protects PP00 from a hung condition.

Multi PP Arithmetic Unit Test

This test is the same as the Arithmetic Unit Test described previously, but runs in PP01 through PP04 simultaneously. If an error is detected, the PP in which the test is running stops and P register stop lights will be the same as for the Arithmetic Unit Test. PP00 is in a loop waiting for a message from PPx indicating the test successfully passed. The looping address is unique to each PP. Each PP is force-deadstarted, waits for the channel 13 flag to set before starting, and sets the channel 12 flag when completed.

LDX Bit Test

This test checks the LDX bit in the maintenance register. If the bit is clear, PP00 stops and the P register indicates an error in the maintenance register.

LDX Error Tables

Tables 5-1 through 5-20 are for isolation of IOU deadstart problems. The purpose of these tables is to relate LDX error stops to suspected faulty modules.

When the IOU will not deadstart or when the LDX tests stop, start troubleshooting by using the LDX error tables. Read the PP register (A, P, Q, and K) values and find the corresponding value for the P register in the LDX error tables. For a given P, the suspected failing modules' codes are listed on the same line. These codes should be used to reference table 5-21 to find the module type and location for the value of the PP reconfiguration.

Table 5-1. I/O Hang Stops

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0025	0024	0500	xxxxxx ¹	KR, KB, HW

Note:

1. A=failing bits (358=failing pattern, 368=failing address).

Table 5-2. Stops for Channel Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0130	0130	0300	xxxxxx ¹	HL, HW, KR, KB
0131	0131	0300	xxxxxx ¹	HL, HW, KR, KB
0132	0132	0300	xxxxxx ¹	HL, HW, KR, KB
0133	0133	0300	xxxxxx ¹	HL, HW, KR, KB
0134	0134	0300	xxxxxx ¹	HL, HW, KR, KB
0147	0147	0300	xxxxxx	HM, HW
0167	0167	0300	xxxxxx	HM, HW
0170	0170	0300	xxxxxx ²	HL, HW, KR, HM
			000000 ²	HL, HW, KR, HM
0171	0171	0300	xxxxxx ²	HL, HW, KR, HM
			000000 ²	HL, HW, KR, HM
0172	0172	0300	xxxxxx ²	HL, HW, KR, HM
			000000 ²	HL, HW, KR, HM
0173	0173	0300	xxxxxx ²	HL, HW, KR, HM
			000000 ²	HL, HW, KR, HM
0174	0174	0300	xxxxxx ²	HL, HW, KR, HM
			000000 ²	HL, HW, KR, HM

Notes:

1. A=channel status errors.

2. A=0 indicates parity error. A≠0 indicates data error (758=expected data, 768=received data).

Table 5-3. Stops for Block Transfer Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0202	0202	0300	xxxxxx ¹ 034343	KB, KR, HW HW, KR

Note:

1. Timeout error (A=0) or failing bits.

Table 5-4. Stops for Conversion Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0226	0226	0300	xxxxxx ¹	HW, KB, KR

1. Timeout error (A=0) or failing bits.

Table 5-5. Stops for PP Memory Errors

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
0211	0211	0300	xxxxxx ¹	KB, KR, HW
0212	0212	0300	xxxxxx ¹	KB, KR, HW
0213	0213	0300	xxxxxx ¹	KB, KR, HW
0214	0214	0300	xxxxxx ¹	KB, KR, HW

Note:

1. Failing bits.

Table 5-6. Arithmetic Unit Error Stops Unconditional Jump Error Stops

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6000	6000	0000	010000	HW, KR, KB
6001	6001	0300	010000	HW, KR, KB
6004	6004	0300	010000	HW, KR, KB
6005	6005	0300	010000	HW, KR, KB
6010	6010	0300	010000	HW, KR, KB
6012	6012	0300	010000	HW, KR, KB
6013	6013	0300	010000	HW, KR, KB
6014	6014	0300	010000	HW, KR, KB
6015	6015	0300	010000	HW, KR, KB
6016	6016	0300	010000	HW, KR, KB
6020	6020	0300	010000	HW, KR, KB
6021	6021	0300	010000	HW, KR, KB
6022	6022	0300	010000	HW, KR, KB
6023	6023	0300	010000	HW, KR, KB
6024	6024	0300	010000	HW, KR, KB
6025	6025	0300	010000	HW, KR, KB
6026	6026	0300	010000	HW, KR, KB
6027	6027	0300	010000	HW, KR, KB
6030	6030	0300	010000	HW, KR, KB
6031	6031	0300	010000	HW, KR, KB
6033	6033	0300	010000	HW, KR, KB
6034	6034	0300	010000	HW, KR, KB
6036	6036	0300	010000	HW, KR, KB
6037	6037	0300	010000	HW, KR, KB
6041	6041	0300	010000	HW, KR, KB
6042	6042	0300	010000	HW, KR, KB
6043	6043	0300	010000	HW, KR, KB
6045	6045	0300	010000	HW, KR, KB
6046	6046	0300	010000	HW, KR, KB
6050	6050	0300	010000	HW, KR, KB
6053	6053	0300	010000	HW, KR, KB
6054	6054	0300	010000	HW, KR, KB
6055	6055	0300	010000	HW, KR, KB
6056	6056	0300	010000	HW, KR, KB
6060	6060	0300	010000	HW, KR, KB
6061	6061	0300	010000	HW, KR, KB
6062	6062	0300	010000	HW, KR, KB
6066	6066	0300	010000	HW, KR, KB
6067	6067	0300	010000	HW, KR, KB
6071	6071	0300	010000	HW, KR, KB
6072	6072	0300	010000	HW, KR, KB
6074	6074	0300	010000	HW, KR, KB
6075	6075	0300	010000	HW, KR, KB
6077	6077	0300	010000	HW, KR, KB
6100	6100	0300	010000	HW, KR, KB
6102	6102	0300	010000	HW, KR, KB
6103	6103	0300	010000	HW, KR, KB
6105	6105	0300	010000	HW, KR, KB
6106	6106	0300	010000	HW, KR, KB

(Continued)

Table 5-6. Arithmetic Unit Error Stops Unconditional Jump Error Stops
(Continued)

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6110	6110	0300	010000	HW, KR, KB
6111	6111	0300	010000	HW, KR, KB
6113	6113	0300	010000	HW, KR, KB
6114	6114	0300	010000	HW, KR, KB
6116	6116	0300	010000	HW, KR, KB
6117	6117	0300	010000	HW, KR, KB
6121	6121	0300	010000	HW, KR, KB
6122	6122	0300	010000	HW, KR, KB
6124	6124	0300	010000	HW, KR, KB
6125	6125	0300	010000	HW, KR, KB
6127	6127	0300	010000	HW, KR, KB
6130	6130	0300	010000	HW, KR, KB
6132	6132	0300	010000	HW, KR, KB
6133	6133	0300	010000	HW, KR, KB
6135	6135	0300	010000	HW, KR, KB
6140	6140	0300	010000	HW, KR, KB
6141	6141	0300	010000	HW, KR, KB
6143	6143	0300	010000	HW, KR, KB
6145	6145	0300	010000	HW, KR, KB
6146	6146	0300	010000	HW, KR, KB
6147	6147	0300	010000	HW, KR, KB
6150	6150	0300	010000	HW, KR, KB
6151	6151	0300	010000	HW, KR, KB
6153	6153	0300	010000	HW, KR, KB
6154	6154	0300	010000	HW, KR, KB
6155	6155	0300	010000	HW, KR, KB
6156	6156	0300	010000	HW, KR, KB
6157	6157	0300	010000	HW, KR, KB
6162	6162	0300	010000	HW, KR, KB
6163	6163	0300	010000	HW, KR, KB
6165	6165	0300	010000	HW, KR, KB
6166	6166	0300	010000	HW, KR, KB
6170	6170	0300	010000	HW, KR, KB
6171	6171	0300	010000	HW, KR, KB
6172	6172	0300	010000	HW, KR, KB
6173	6173	0300	010000	HW, KR, KB
6176	6176	0300	010000	HW, KR, KB
6177	6177	0300	010000	HW, KR, KB
6201	6201	0300	010000	HW, KR, KB

Table 5-7. Conditional Jump Error Stops

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6203	6202	1400	xxxxxxx	HW, KR, KB
6204	6203	0700	xxxxxxx	HW, KR, KB
6205	6204	0500	xxxxxxx	HW, KR, KB
6206	6206	0300	000000	HW, KR, KB
6207	6207	0300	010000	HW, KR, KB
6211	6211	0300	000000	HW, KR, KB
6214	6213	0700	000001	HW, KR, KB
6215	6214	0400	000000	HW, KR, KB
6216	6216	0300	000001	HW, KR, KB
6220	6220	0300	000001	HW, KR, KB
6222	6221	1500	xxxxxxx	HW, KR, KB
6223	6222	0600	xxxxxxx	HW, KR, KB
6224	6224	0300	777777	HW, KR, KB

Table 5-8. Error Stops for 1x and 2x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6226	6225	1600	xxxxxxx	HW, KR
6227	6226	0500	xxxxxxx	KR, HW
6230	6230	0300	000000	KR, HW
6233	6232	0400	000000	KR, HW
6235	6234	0400	000000	KR, HW
6237	6236	0400	000000	KR, HW
6241	6240	0400	000000	KR, HW
6243	6242	0400	000000	KR, HW
6245	6244	1700	xxxxxxx	HW, KR
6246	6245	0500	xxxxxxx	KR, HW
6251	6250	0500	xxxxxxx	KR, HW
6261	6260	0500	xxxxxxx	KR, HW
6271	6270	0500	xxxxxxx	KR, HW
6272	6271	1100	xxxxxxx	HW, KR
6274	6273	0500	xxxxxxx	KR, HW
6300	6277	0500	xxxxxxx	KR, HW
6302	6301	1200	xxxxxxx	KR, HW
6303	6302	0500	xxxxxxx	KR, HW
6307	6306	0500	xxxxxxx	KR, HW
6311	6310	1300	xxxxxxx	HW, KR
6312	6311	0500	xxxxxxx	KR, HW
6315	6314	0500	xxxxxxx	KR, HW
6317	6316	1000	xxxxxxx	HW, KR
6322	6321	0500	xxxxxxx	KR, HW
6327	6326	0500	xxxxxxx	KR, HW
6330	6327	2400	xxxxxxx	HW, KR
6331	6330	2500	xxxxxxx	HW, KR
6332	6331	2000	xxxxxxx	HW, KR
6334	6333	0500	xxxxxxx	KR, HW

(Continued)

Table 5-8. Error Stops for 1x and 2x Instructions (Continued)

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6337	6336	0400	000000	KR, HW
6342	6341	0400	000000	KR, HW
6345	6344	0400	000000	KR, HW
6350	6347	0400	000000	KR, HW
6353	6352	0400	000000	KR, HW
6356	6355	0400	000000	KR, HW
6361	6360	0400	000000	KR, HW
6364	6363	0400	000000	KR, HW
6367	6366	0400	000000	KR, HW
6372	6371	0400	000000	KR, HW
6375	6374	0400	000000	KR, HW
6400	6377	0400	000000	KR, HW
6403	6402	2100	xxxxxx	HW, KR
6405	6404	0500	xxxxxx	KR, HW
6406	6405	2300	xxxxxx	HW, KR
6410	6407	0600	xxxxxx	KR, HW
6412	6411	0500	xxxxxx	KR, HW
6413	6412	2200	xxxxxx	HW, KR
6417	6416	0500	xxxxxx	KR, HW
6425	6424	0500	xxxxxx	KR, HW
6433	6432	0500	xxxxxx	KR, HW
6441	6440	0500	xxxxxx	KR, HW
6447	6446	0500	xxxxxx	KR, HW
6474	6473	0500	xxxxxx	KR, HW
6506	6505	0400	xxxxxx	KR, HW
6510	6507	0500	xxxxxx	KR, HW

Table 5-9. Error Stops for 3x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6511	6510	3400	xxxxxx	HW, KR
6516	6515	3000	xxxxxx	HW, KR
6517	6516	0500	xxxxxx	KB, KR
6521	6520	0400	xxxxxx	KB, KR
6522	6521	3100	xxxxxx	HW, KR
6525	6524	0500	xxxxxx	KB, KR
6527	6526	3200	xxxxxx	HW, KR
6531	6530	0500	xxxxxx	KB, KR
6533	6532	3300	xxxxxx	HW, KR
6535	6534	0500	xxxxxx	KB, KR
6537	6536	3500	xxxxxx	HW, KR
6541	6540	0500	xxxxxx	KB, KR
6552	6551	0500	xxxxxx	KB, KR
6553	6552	3600	xxxxxx	HW, KR
6554	6553	3700	xxxxxx	HW, KR

Table 5-10. Error Stops for 4x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6563	6562	4400	xxxxxxx	HW, KR
6566	6565	4000	xxxxxxx	HW, KR
6570	6567	0500	xxxxxxx	KR, KB
6572	6571	4100	xxxxxxx	HW, KR
6573	6572	0500	xxxxxxx	KR, KB
6574	6573	4200	xxxxxxx	HW, KR
6576	6575	0500	xxxxxxx	KR, KB
6577	6576	4300	xxxxxxx	HW, KR
6601	6600	0500	xxxxxxx	KR, KB
6602	6601	4600	xxxxxxx	HW, KR
6606	6606	0300	xxxxxxx	KR, KB
6611	6610	4700	xxxxxxx	HW, KR
6614	6613	0500	xxxxxxx	KR, KB
6616	6615	4500	xxxxxxx	HW, KR
6624	6623	0500	xxxxxxx	KR, KB

Table 5-11. Error Stops for 5x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6631	6630	5000	xxxxxxx	HW, KR
6633	6632	5400	xxxxxxx	HW, KR
6637	6636	0500	xxxxxxx	KR, KB
6641	6640	5100	xxxxxxx	HW, KR
6643	6642	0500	xxxxxxx	KR, KB
6644	6643	5200	xxxxxxx	HW, KR
6647	6646	0500	xxxxxxx	KR, KB
6650	6647	5300	xxxxxxx	HW, KR
6653	6652	0500	xxxxxxx	KR, KB
6656	6656	0300	xxxxxxx	HW, KR
6662	6661	5500	xxxxxxx	KR, KB
6671	6670	0500	xxxxxxx	KR, KB
6672	6671	5600	xxxxxxx	HW, KR
6701	6700	0500	xxxxxxx	KR, KB
6702	6701	5700	xxxxxxx	HW, KR
6711	6710	0500	xxxxxxx	KR, KB

Table 5-12. Error Stops for 13x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
6720	6717	103400	xxxxxx	HW, KR
6723	6722	103000	xxxxxx	HW, KR
6726	6725	000500	xxxxxx	KB, KR
6727	6726	103100	xxxxxx	HW, KR
6732	6731	000500	xxxxxx	KB, KR
6734	6733	103200	xxxxxx	HW, KR
6735	6734	000500	xxxxxx	KB, KR
6737	6736	102200	xxxxxx	HW, KR
6741	6740	000500	xxxxxx	KB, KR
6743	6742	103300	xxxxxx	HW, KR
6744	6744	000300	xxxxxx	KB, KR
6747	6746	103600	xxxxxx	HW, KR
6755	6754	000500	xxxxxx	KB, KR
6756	6755	103700	xxxxxx	HW, KR
6763	6762	000500	xxxxxx	KB, KR
6765	6764	103500	xxxxxx	HW, KR
6773	6772	000500	xxxxxx	KB, KR

Table 5-13. Error Stops for 14x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7005	7004	104400	xxxxxx	HW, KR
7007	7006	104000	xxxxxx	HW, KR
7011	7010	000500	xxxxxx	KR, KB
7012	7011	104100	xxxxxx	HW, KR
7014	7013	000500	xxxxxx	KR, KB
7016	7015	104200	xxxxxx	HW, KR
7017	7016	000500	xxxxxx	KR, KB
7021	7020	102300	xxxxxx	HW, KR
7023	7022	000500	xxxxxx	KR, KB
7025	7024	104300	xxxxxx	HW, KR
7026	7026	000300	xxxxxx	KR, KB
7031	7030	104600	xxxxxx	HW, KR
7037	7036	000500	xxxxxx	KR, KB
7040	7037	104700	xxxxxx	HW, KR
7045	7044	000500	xxxxxx	KR, KB
7047	7046	104500	xxxxxx	HW, KR
7055	7054	000500	xxxxxx	KR, KB

Table 5-14. Error Stops for 15x Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7062	7061	105000	xxxxxx	HW, KR
7065	7064	000500	xxxxxx	KR, KB
7067	7066	105400	xxxxxx	HW, KR
7073	7072	000500	xxxxxx	KR, KB
7074	7073	105100	xxxxxx	HW, KR
7077	7076	000500	xxxxxx	KR, KB
7101	7100	102400	xxxxxx	HW, KR
7104	7103	000500	xxxxxx	KR, KB
7106	7105	105200	xxxxxx	HW, KR
7110	7107	000500	xxxxxx	KR, KB
7112	7111	105300	xxxxxx	HW, KR
7114	7114	000300	xxxxxx	KR, KB
7117	7116	105600	xxxxxx	HW, KR
7126	7125	000500	xxxxxx	KR, KB
7127	7126	105700	xxxxxx	HW, KR
7136	7135	000500	xxxxxx	KR, KB
7140	7137	105500	xxxxxx	HW, KR
7147	7146	000500	xxxxxx	KR, KB

Table 5-15. Error Stops for 01 and 02 Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7164	7164	0300	xxxxxx	HW, KR, KB
7362	7362	0300	xxxxxx	HW, KR, KB
7363	7363	0300	xxxxxx	HW, KR, KB
7402	7402	0300	xxxxxx	HW, KR, KB

Table 5-16. Error Stops for IOU Instructions

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7410	0014	006400	xxxxxx	HW, KR, KB
7411	7411	000300	xxxxxx	HW, HM
7413	0014	006500	xxxxxx	HW, KR, KB
7415	0014	006600	xxxxxx	HW, KR, KB
7416	7416	000300	xxxxxx	HW, HM
7420	0014	006700	xxxxxx	HW, KR, KB
7422	0014	106400	xxxxxx	HW, KR, KB
7423	7423	000300	xxxxxx	HW, HM
7425	0014	106500	xxxxxx	HW, KR, KB

Table 5-17. Error Stops for Multiple PP Arithmetic Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7627	0012	106500	xxxxxxx	HW, KR

Table 5-18. Error Stops for Escape Bit Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7637	0012	7500	xxxxxxx	HW, HL, KR
7641	0012	7200	xxxxxxx	HW, HL, KR
7642	0012	7000	xxxxxxx	HW, HL, KR
7643	7642	0500	xxxxxxx	HW, HL, KR
7644	0000	7300	xxxxxxx	HW, HL, KR
7646	7645	0500	xxxxxxx	HW, HL, KR
7647	0012	7100	xxxxxxx	HW, HL, KR
7651	7650	0500	xxxxxxx	HW, HL, KR
7652	0012	7400	xxxxxxx	HW, HL, KR
7654	0012	7600	xxxxxxx	HW, HL, KR
7655	0012	7700	xxxxxxx	HW, HL, KR
7657	0012	6600	xxxxxxx	HW, HL, KR

Table 5-19. Error Stops for LDX Bit in MR Test

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7715	0017	7500	xxxxxxx	HM, HW, HC, HS, HQ
7716	0017	7700	xxxxxxx	HM, HW, HC, HS, HQ
7722	0017	7100	xxxxxxx	HM, HW, HC, HS, HQ
7724	0017	7500	xxxxxxx	HM, HW, HC, HS, HQ
7665	0017	7400	000000	HM, HW, HC, HS, HQ
7671	7670	0400	000000	HM, HW, HC, HS, HQ

Table 5-20. Error Stops for MAC Access

P Rgtr	Q Rgtr	K Rgtr	A Rgtr	Suspected Failing Module(s)
7763	0017	7400	xxxxxxx	HW, HM, HQ
7766	0017	7500	xxxxxxx	HW, HM, HQ

Module Location

Module locations are listed in table 5-21. Since there is no barrel reconfiguration, all modules are always in the same locations.

Table 5-21. IOU Module Locations

Module Code	Module	Bar0 ¹	Bar1 ¹	Bar2 ¹	Bar3 ¹	Comment
HW	1HWH	B15	A17	D17	C17	Microcode and conversion module
KR	1KRH	B16	A18	D18	C18	P, Q, K, and A registers
KB	1KBH	B17	A19	D19	C19	PP memory module
HC	1HCH	A24	A24	C24	C24	CM address and PP MAC control
HK	1HKH	B20	B20	B20	B20	TPM Module
HS	1HSH	B18	B18	D21	D21	Maintenance register A module
HT	1HTH	A21	A21	C21	C21	Maintenance register B module
HQ	1HQH	B01	B01	B01	B01	MAC module
HA	1HAH	A20	A20	C20	C20	Master clock module
HM	1HMH	B02	B02	B02	B02	Maintenance channels (15,17)
HL00	1HLH	B03	B03	B03	B03	Channels 0, 1, 12, 13

Note:

1. Module location.

Power Distribution and Warning System Troubleshooting

6

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Power Distribution and Warning System Troubleshooting

6

This chapter provides troubleshooting information for the power distribution and warning system. For additional information, refer to the Power and Environmental Subsystems Hardware Maintenance manual. This chapter lists possible causes of coded fault messages. The power unit displays a coded fault message when an early environmental warning (EEW), long warning (LW), or short warning (SW) is issued or an immediate shutdown has occurred. EEW does not shut the system down, LW shuts the system down in 2 minutes (1 minute for IOU faults), and SW shuts the system down in 2.5 seconds.

If an immediate shutdown has occurred, do not attempt a restart until the fault has been found and corrected. Coded fault messages can still be displayed if 50/60-Hz power is present at the power unit. Ensure that the 50/60-Hz and 400-Hz DISCONNECT circuit breakers behind rear door of power unit are reset.

Displaying Coded Fault Messages at Power Unit

To observe coded fault messages, perform the following procedure.

1. Using 5/16-in Allen wrench, loosen retainers on front door of power unit and open door.
2. Set Selector (left) rotary switch below DATA display to AUX.
3. Set Function (right) rotary switch below DATA display to MSG. This enables a two-, three-, or four-character code in MESSAGE portion of alphanumeric display. If more than one fault has been detected, separate codes display alternately for each fault.

Normal Operation

The three-character display AAA indicates no errors have occurred.

Monitor Board Errors

All three- and four-character displays except AAA (normal operation) indicate errors caused by a defective monitor board.

Environment Errors

All two-character displays indicate an environment error. Table 6-1 lists possible causes for the coded fault messages displayed on the power unit.

NOTE

The number 6 and the letter b are similar. The 6 has a square top, the b does not.

Table 6-1. Two-Character Coded Fault Messages

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
00	LW (2 min)	Invalid temperature indication from -2.0-V power supply heat sink sensor in power unit.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
03	LW (2 min)	Invalid temperature indication from -4.5-V power supply heat sink sensor in power unit.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
06	LW (2 min)	Invalid temperature indication from CP-0 shunt sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
09	LW (2 min)	Invalid temperature indication from CP-1 shunt sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
0C	SW	Invalid temperature indication from CP-0 outlet sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
0F	SW	Invalid temperature indication from CP-1 outlet sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
12	SW	Invalid temperature indication from memory 1 outlet sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
15	LW (2 min)	Temperature at -2.0-V power supply heat sink in power unit exceeds 93°C (200°F).	1. -2V power supply shorted internally. 2. Faulty blower in power unit. 3. Restricted airflow.	2

Notes:

1. Reading from sensor is out of acceptable range of -4 to 121°C (25 to 250°F).
2. Results in an emergency shutdown of logic voltages to CPU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
18	LW (2 min)	Invalid temperature indication from memory 2 outlet sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
1b	LW (2 min)	Invalid temperature indication from CP ambient sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
1E	LW (2 min)	Invalid temperature indication from CM ambient sensor in CPU.	1. Cable disconnected from sensor. 2. Sensor shorted.	1,2
21	LW (2 min)	Invalid temperature indication from reverse airflow sensor in CPU.	Faulty blower in CM.	1,2
27	LW (2 min)	Temperature at -4.5-V power supply heat sink in power unit exceeds 93°C (200°F).	1. -4.5V power supply shorted internally. 2. Faulty blower in power unit. 3. Restricted airflow.	2
2A	EEW	Temperature at CP-0 shunt sensor in CPU exceeds 55°C (131°F).	1. Restricted airflow due to clogged filter or obstructed inlet to CPU blower. 2. Room ambient temp too high. 3. System is improperly positioned and recycles its own heat.	

Notes:

1. Reading from sensor is out of acceptable range of -4 to 121°C (25 to 250°F).

2. Results in an emergency shutdown of logic voltages to CPU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
2d	LW (2 min)	Temperature at CP-0 shunt sensor in CPU exceeds 60°C (140°F).	1. CPU blower is stopped. 2. CPU blower is single phasing and running too slowly.	1
30	SW	Temperature at CP-0 shunt sensor in CPU exceeds 63°C (145°F).	1. CPU blower is stopped. 2. CPU blower is single phasing and running too slowly.	2
33	EEW	Temperature at CP-1 shunt sensor in CPU exceeds 55°C (131°F).	1. Restricted airflow due to clogged filter or obstructed inlet to CPU blower. 2. Room ambient temp too high. 3. System is improperly positioned and recycles its own heat.	
36	LW (2 min)	Temperature at CP-1 shunt sensor in CPU exceeds 60°C (140°F).	1. CPU blower is stopped. 2. CPU blower is single phasing and running too slowly.	2
39	SW	Temperature at CP-1 shunt sensor in CPU exceeds 63°C (145°F).	1. CPU blower is stopped. 2. CPU blower is single phasing and running too slowly.	2
3C	EEW	Temperature of room ambient air exceeds 32°C (89°F).	Room temp too high.	1

Notes:

1. Temperature of room ambient air is average between temperatures from CP and CM ambient sensors.

2. Results in an emergency shutdown of logic voltages to CPU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
3F	LW (2 min)	Temperature of room ambient air exceeds 34°C (93°F).	Room temp too high.	1,2
42	SW	CP-0 outlet temperature exceeds CP ambient temperature by more than 18°C (32°F).	1. CPU blower is stopped. 2. Extremely restricted airflow.	3
45	SW	CP-1 outlet temperature exceeds CP ambient temperature by more than 18°C (32°F).	1. CPU blower is stopped. 2. Extremely restricted air flow.	3
48	SW	Memory 1 outlet temperature exceeds CM ambient temperature by more than 18°C (32°F).	1. CM blower is stopped. 2. Extremely restricted air flow.	3
4b	SW	Memory 2 outlet temperature exceeds CM ambient temperature by more than 18°C (32°F).	1. CM blower is stopped. 2. Extremely restricted air flow.	3
4E	SW	Reverse airflow temperature exceeds CM ambient temperature by more than 7°C (14°F).	1. CM blower is stopped. 2. Extremely restricted air flow.	3
51	None	Overcurrent of 529 A on -2.0-V power supply output to CP-0.	1. Sense wire or cable disconnected. 2. Dead short on -2.0V bus.	3,4

Notes:

1. Temperature of room ambient air is average between temperatures from CP and CM ambient sensors.
2. Results in an emergency shutdown of system if fault continues to end of warning time.
3. Results in an emergency shutdown of logic voltages to CPU if fault continues to end of warning time.
4. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
54	None	Overcurrent of 464 A on -2.0-V power supply output to CP-1.	1. Sense wire or cable disconnected. 2. Dead short on -2.0V bus.	1,2
57	None	Overcurrent of 111 A on -2.0-V power supply output to CM.	1. Sense wire or cable disconnected. 2. Dead short on -2.0V bus. 3. Common connector for -2.0V and +5.0V power supplies disconnected.	1,2
5A	None	Overcurrent of 912 A on -4.5-V power supply output to CP-0.	1. Sense wire or cable disconnected. 2. Dead short on -4.5V bus.	1,2
5d	None	Overcurrent of 912 A on -4.5-V power supply output to CP-1.	1. Sense wire or cable disconnected. 2. Dead short on -4.5V bus.	1,2
60	None	Overcurrent of 270 A on -4.5-V power supply output to CM.	1. Sense wire or cable disconnected. 2. Dead short on -4.5V bus.	1,2

Notes:

1. Results in an immediate emergency shutdown of logic voltages to CPU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
63	None	Overcurrent of 117 or 167 A on +5.0-V power supply output to CM.	1. Sense wire or cable disconnected. 2. Dead short on +5.0V bus. 3. Common connector for -2.0V and +5.0V regulators disconnected.	1,2,3
66	None	Logic cage interlock for CP-0 is open.	1. Logic board not installed properly. 2. Logic board missing. 3. Cable disconnected. 4. If CP-1 not present, jumper plug at bottom of CP-1 area missing.	1
69	None	Logic cage interlock for CP-1 is open.	1. Logic board not installed properly. 2. Logic board missing. 3. Cable disconnected.	1
6C	None	Overvoltage of -2.3 V on -2.0-V power supply output to CPU.	1. Disconnected cable. 2. Momentary short on -2.0V bus. 3. Variac adjusted too high. 4. Voltage surge on -2.0V bus.	1,2

Notes:

1. Results in an immediate emergency shutdown of logic voltages to CPU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.
3. Overcurrent of 117 A applies if S1 switches on CM regulator modules are in C1 position (eight or less memory modules in CM). Overcurrent of 167 A applies if S1 switches are in C2 position (more than eight memory modules in CM).

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
6F	None	Overvoltage of -5.1 V on -4.5-V power supply output to CPU.	1. Disconnected cable. 2. Momentary short on -4.5V bus. 3. Variac adjusted too high. 4. Voltage surge on -4.5V bus.	1,2
72	None	Overvoltage of +5.7 V on +5.0-V power supply output to CPU.	1. Disconnected cable. 2. Momentary short on +5.0V bus. 3. Variac adjusted too high. 4. Voltage surge on +5.0V bus.	1,2
75	SW	Blower motor for CP has overheated.	1. Blower cable disconnected at CP interface. 2. Blower motor thermostat cable is open. 3. Blower motor is single phasing or has other internal damage. 4. Obstruction lodged in blower. 5. Blower motor thermostat is open. 6. Restricted airflow to blower motor.	3

Notes:

1. Results in an immediate emergency shutdown of logic voltages to CPU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.
3. Results in an emergency shutdown of logic voltages to CPU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
78	SW	Blower motor for CM has overheated.	1. Blower cable disconnected at CM interface. 2. Blower motor thermostat cable is open. 3. Blower motor is single phasing or has other internal damage. 4. Obstruction lodged in blower. 5. Blower motor thermostat is open. 6. Restricted airflow to blower motor.	¹
7b	SW	Blower motor for power unit has overheated.	1. Blower cable disconnected at power unit interface. 2. Blower motor thermostat cable is open. 3. Blower motor is single phasing or has other internal damage. 4. Obstruction lodged in blower. 5. Blower motor thermostat is open. 6. Restricted airflow to blower motor.	¹

Notes:

1. Results in an emergency shutdown of logic voltages to CPU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages *(Continued)*

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
7E	None	One or more power supply circuit breaker(s) are off in power unit.	1. Any of these circuit breakers tripped. 2. Any of these circuit breakers is defective. 3. Open wire connecting these circuit breakers in series.	¹
81	SW	Power from MG 1 will be lost in 2.5 seconds unless power interruption to MG is momentary.	1. Faulty MG 1 2. Faulty MG interface unit. 3. Defective cable between MG 1 and MG interface unit. 4. Defective cable between MG interface unit and power unit. 5. Open wire from power control board to connector in power unit.	²

Notes:

1. Results in an immediate emergency shutdown of logic voltages to CPU.
2. Results in an emergency shutdown of system if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
84	SW	Power from MG 2 will be lost in 2.5 seconds unless power interruption to MG is momentary.	1. Faulty MG 2 2. Faulty MG interface unit. 3. Defective cable between MG 2 and MG interface unit. 4. Defective cable between MG interface unit and power unit. 5. Open wire from power control board to connector in power unit. 6. Variac adjusted too high.	1
87	None	Remote start/warning cable chain to IOUs (from J8 in CPU to J41/J40 in IOUs and back to J7 in CPU) is disconnected at some point.	Cable disconnected.	2
8A	LW (2 min)	Power unit has initiated a LW (this indication accompanies code for LW fault).	Refer to LW possible causes.	
8d	SW	Power unit has initiated a SW (this indication accompanies code for SW fault).	Refer to SW possible causes.	

Notes:

1. Results in an emergency shutdown of system if fault continues to end of warning time.

2. Results in an immediate emergency shutdown of logic voltages to CPU.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
90	None	One or more power supply circuit breakers in standard IOU are off.	1. Circuit breaker tripped. 2. Overvoltage/current condition described for codes A5, A8, and Ab.	1
93	None	One or more power supply circuit breakers in IOU expansion are off.	1. Circuit breaker tripped. 2. Overvoltage/current condition described for codes b7, bA, and bd.	1
96	None	One or more power supply circuit breakers in standalone IOU are off.	1. Circuit breaker tripped. 2. Overvoltage/current condition described for codes C9, CC, and CF.	1
99	None	One or more power supply circuit breakers in standalone IOU expansion are off.	1. Circuit breaker tripped. 2. Overvoltage/current condition described for codes db, dE, and E1.	1
9C	LW (1 min)	Temperature at 1TS2 or 1TS3 sensor on power heat sink in standard IOU exceeds 83°C (180°F).	1. Blocked air vent. 2. Faulty temp sensor. 3. IOU blower failing. 4. Faulty power control board.	2

Notes:

1. Results in an immediate emergency shutdown of logic voltages in affected IOU.
2. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
9F	LW (1 min)	Blower in standard IOU has stopped.	1. Loss of 50/60-Hz power. 2. Faulty blower in IOU. 3. 50/60-Hz circuit breaker tripped.	1
A2	None	Temperature at backup 1S1 or 1S2 thermostat on power heat sink in standard IOU exceeds 83°C (180°F).	1. Room temp too high. 2. Blocked airflow near thermostats. 3. No 50/60 Hz to IOU blower. 4. Blower is stopped. 5. Faulty thermostat. 6. Faulty power control board.	2,3
A5	None	Overvoltage/overcurrent of -6.0 ± 0.6 V/750 A on V2 (-5.2-V) power supply output in standard IOU.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	2,4

Notes:

1. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.
2. Results in an immediate emergency shutdown of logic voltages to IOU.
3. All power supply CBs (V1 - V3 DISCONNECT) are tripped on affected IOU.
4. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
A8	None	Overvoltage/overcurrent of -2.6 ± 0.3 V/400 A on V1 (-2.2-V) power supply output in standard IOU.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
Ab	None	Overvoltage/overcurrent of $+5.82 \pm 0.58$ V/400 A on V3 (-5.0-V) power supply output in standard IOU.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
AE	LW (1 min)	Temperature at 1TS2 or 1TS3 sensor on power heat sink in IOU expansion exceeds 83°C (180°F).	1. Blocked air vent. 2. Faulty temp sensor. 3. IOU blower failing. 4. Faulty power control board.	3

Notes:

1. Results in an immediate emergency shutdown of logic voltages in affected IOU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.
3. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
b1	LW (1 min)	Blower in IOU expansion has stopped.	1. Loss of 50/60-Hz power. 2. Faulty blower in IOU. 3. 50/60-Hz circuit breaker tripped.	1
b4	None	Temperature at backup 1S1 or 1S2 thermostat on power heat sink in IOU expansion exceeds 83°C (180°F).	1. Room temp too high. 2. Blocked airflow near thermostats. 3. No 50/60 Hz to IOU blower. 4. Blower is stopped. 5. Faulty thermostat. 6. Faulty power control board.	2,3
b7	None	Overvoltage/overcurrent of -6.0 ± 0.6 V/750 A on V2 (-5.2-V) power supply output in IOU expansion.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	2,4

Notes:

1. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.
2. Results in an immediate emergency shutdown of logic voltages in affected IOU.
3. All power supply CBs (V1 - V3 DISCONNECT) are tripped on affected IOU.
4. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
bA	None	Overvoltage/overcurrent of -2.6 ± 0.3 V/400 A on V1 (-2.2 -V) power supply output in IOU expansion.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
bd	None	Overvoltage/overcurrent of $+5.82 \pm 0.58$ V/400 A on V3 ($+5.0$ -V) power supply output in IOU expansion.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
C0	LW (1 min)	Temperature at 1TS2 or 1TS3 sensor on power heat sink in standalone IOU exceeds 83°C (180°F).	1. Blocked air vent. 2. Faulty temp sensor. 3. IOU blower failing. 4. Faulty power control board.	3

Notes:

1. Results in an immediate emergency shutdown of logic voltages in affected IOU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.
3. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
C3	LW (1 min)	Blower in standalone IOU has stopped.	1. Loss of 50/60-Hz power. 2. Faulty blower in IOU. 3. 50/60-Hz circuit breaker tripped.	1
C6	None	Temperature at backup 1S1 or 1S2 thermostat on power heat sink in standalone IOU exceeds 83°C (180°F).	1. Room temp too high. 2. Blocked airflow near thermostats. 3. No 50/60 Hz to IOU blower. 4. Blower is stopped. 5. Faulty thermostat. 6. Faulty power control board.	2,3
C9	None	Overvoltage/overcurrent of -6.0 ± 0.6 V/750 A on V2 (-5.2-V) power supply output in standalone IOU.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	2,4

Notes:

1. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.
2. Results in an immediate emergency shutdown of logic voltages in affected IOU.
3. All power supply CBs (V1 - V3 DISCONNECT) are tripped on affected IOU.
4. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
CC	None	Overvoltage/overcurrent of -2.6 ± 0.3 V/400 A on V1 (-2.2-V) power supply output in standalone IOU.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
CF	None	Overvoltage/overcurrent of $+5.82 \pm 0.58$ V/400 A on V3 (+5.0-V) power supply output in standalone IOU.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
d2	LW (1 min)	Temperature at 1TS2 or 1TS3 sensor on power heat sink in standalone IOU expansion exceeds 83°C (180°F).	1. Blocked air vent. 2. Faulty temp sensor. 3. IOU blower failing. 4. Faulty power control board.	3

Notes:

1. Results in an immediate emergency shutdown of logic voltages in affected IOU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.
3. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
d5	LW (1 min)	Blower in standalone IOU expansion has stopped.	1. Loss of 50/60-Hz power. 2. Faulty blower in IOU. 3. 50/60-Hz circuit breaker tripped.	1
d8	None	Temperature at backup 1S1 or 1S2 thermostat on power heat sink in standalone IOU expansion exceeds 83°C (180°F).	1. Room temp too high. 2. Blocked airflow near thermostats. 3. No 50/60 Hz to IOU blower. 4. Blower is stopped. 5. Faulty thermostat. 6. Faulty power control board.	2,3
db	None	Overvoltage/overcurrent of -6.0 ± 0.6 V/750 A on V2 (-5.2-V) power supply output in standalone IOU expansion.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	2,4

Notes:

1. Results in an emergency shutdown of logic voltages in affected IOU if fault continues to end of warning time.
2. Results in an immediate emergency shutdown of logic voltages in affected IOU.
3. All power supply CBs (V1 - V3 DISCONNECT) are tripped on affected IOU.
4. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

(Continued)

Table 6-1. Two-Character Coded Fault Messages (Continued)

Code Displayed in MESSAGE	Type Warn.	Fault	Possible Causes	Note
dE	None	Overvoltage/overcurrent of -2.6 ± 0.3 V/400 A on V1 (-2.2-V) power supply output in standalone IOU expansion.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2
E1	None	Overvoltage/overcurrent of $+5.82 \pm 0.58$ V/400 A on V3 (+5.0-V) power supply output in standalone IOU expansion.	1. Tool on backpanel. 2. Incorrectly plugged board. 3. Shorted board(s). 4. MG voltage too high. 5. Faulty power control board. 6. Variac adjusted wrong.	1,2

Notes:

1. Results in an immediate emergency shutdown of logic voltages in affected IOU.
2. Circuit breaker of power supply with overcurrent/overvoltage is tripped.

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Maintenance Software Test and Section Index

A

This appendix briefly describes maintenance software tests. A test and section index is provided for:

- IOU Tests (FII40/FII44)
- IOU/CP/CM Model Independent Tests (ALLMI3)
- CP/CM Model Dependent Tests (ALLMD3)

Clock frequency and width margins may be selected while running the tests. Use the MSL command CM for fast (F) or slow (S) frequency and wide (W) or narrow (N) width margins as follows.

Margin	IOU	CM	CP-0
Fast	CM,I,F	CM,M,F	CM,P,F
Slow	CM,I,S	CM,M,S	CM,P,S
Wide	CM,I,W	CM,M,W	CM,P,W
Narrow	CM,I,N	CM,M,N	CM,P,N

Fast/slow margins may be combined with wide/narrow margins. For example: CM,P,FN or CM,P,FW or CM,P,SN OR CM,P,SW.

IOU Tests (FII40/FII44)

These tests assume that LDS and EDS (960) or LDX (962) have run successfully.

The following paragraphs describe the IOU tests in command buffers FII40 (for 960) and FII44 (for 962).

QLT4 - Quicklook Test

The test section number (converted to octal), represents the channel under test.

Section	Description
00	Test one word input/output over channel 00.
01	Test one word input/output over channel 01.
02	Test one word input/output over channel 02.
03	Test one word input/output over channel 03.
04	Test one word input/output over channel 04.
05	Test one word input/output over channel 05.
06	Test one word input/output over channel 06.
07	Test one word input/output over channel 07.
08	Test one word input/output over channel 10.
...	
27	Test one word input/output over channel 33.

PMT4 - PP Memory Test 1

The test section number represents the PP under test.

Section	Description
00	Test PP00 memory.
01	Test PP01 memory.
02	Test PP02 memory.
03	Test PP03 memory.
04	Test PP04 memory.
05	Test PP05 memory.
06	Test PP06 memory.
07	Test PP07 memory.
08	Test PP10 memory.
09	Test PP11 memory.
...	
16	Test PP20 memory.
...	
25	Test PP31 memory.

EXT4 - Execution Unit Test

Sections are not selectable.

Section	Tag	Description
00	UJNTST	Tests arithmetic unit and execution of 12-bit operand instructions 00 through 578.
01	TEST13X	Tests arithmetic unit and execution of 16-bit operand instructions 1030 through 10578.
02	STSTEST	Tests execution of channel instructions.

PMU4 - PP Memory Test 2

Section	Description
00	Executes in lower half of memory; tests all memory except test core and direct cells used by lower-half copy.
01	Executes in upper half of memory; tests direct cells and core used by lower-half copy.

CHD4 - Channel Test

The number of sections selected (0 through 31) specifies the number of channels to be tested for one PP pair.

CMA4 - Central Memory Access Test

Section	Tag	Description
00	SEC00	Tests relocation (R) register.
01	SEC01	Tests (R + A), central memory address.
02	CWDTST	Tests read/write central memory with 60-bit single central memory word.
03	ADRTST	Test read/write addresses in central memory with 60-bit single central memory word.
04	CWMTST	Tests read/write central memory with 64-bit single central memory word.
05	CLDTST	Tests read/write block in central memory with 60-bit central memory word.
06	CLMTST	Tests read/write block in central memory with 64-bit central memory word.
07	RSLTST	Tests read and set lock.
08	RCLTST	Test read and clear lock.
09	MIXTST	Tests read/write in mixed mode 60- and 64-bit central memory word, single central memory word and block.

MRA4 - Maintenance Register Access Test

Sections 1 through 25 represent PP number from which MCH is accessed.

Section	Tag	Description
00	SEC00	Tests MCH interlock and PP priority.
01		Tests MCH access from PP01.
:		
25		Tests MCH access from PP31.

MRT4 - Maintenance Register Test

Section	Tag	Description
00	SEC00	Tests OS bounds violation.
01	SEC01	Tests PP halt on error feature.
02	SEC02	Tests parity networks in barrel 0.
03	SEC03	Tests parity networks in barrel 1.
04	SEC04	Tests parity networks in barrel 2.
05	SEC05	Tests parity networks in barrel 3.
06	SEC06	Tests parity networks in MCH.
07	SEC07	Tests parity networks on channels.
08	SEC10	Tests parity networks on CM access port.
09	SEC11	Tests forcing 1 on data and address parity to CM.

DST4 - Display Alignment Test

DST4 is not part of command buffer FII40/FII44. It can be run individually to test the CC545 display console and controller if used on the 960 (not supported).

Section	Tag	Description
00	SEC00	Tests dot function, CDC display code.
01	SEC01	Tests one character, full screen, CDC display code.
02	SEC02	Tests full alphabet, CDC display code.
03	SEC03	Tests intensity, CDC display code.
04	SEC04	Tests dot function, ASCII code.
05	SEC05	Tests one character, full screen, ASCII.
06	SEC06	Tests full alphabet, ASCII code.
07	SEC07	Tests intensity, ASCII code.

TPM4 - Two-Port Mux Test

TPM4 is not part of command buffer FII40/FII44. It can be run individually to test the two-port mux.

Section	Tag	Description
00	SEC00	Tests function response and FIFO.
01	SEC01	Tests DTR and connect function.
02	SEC02	Displays full alphabet.
03	SEC03	Tests master clear and disconnect function.
04	SEC04	Tests x-y positioning and parity error detection.
05	SEC05	Tests x-y positioning, displays dot code.
06	SEC06	Tests data in overrun.

IOU/CP/CM Model Independent Tests (ALLMI3)

ALLMI3 consists of the 14 model independent tests described in the following paragraphs.

CMEM - Central Memory Test

CMEM is organized into 11 sections to test CM using different data patterns.

Section	CM Pattern
1-5	Five unique data patterns. Data compare operations can be switched on or off.
6	Marching pattern.
7	Addressing pattern where the word address of the word being accessed is used as the data word.
8	Complement of the word addresses in section 7.
9	Five-byte data pattern.
10	Sixteen-word blocks.
11	Randomly-generated data pattern.

RCT1 - Random Command Test

RCT1 contains test passes and conditions. A test pass is the generation of a random set of instructions that are simulated and executed. The simulated results are compared with the actual results. Conditions within each pass are used to insert different types of purge instructions into the first two parcels of the execution list and to insert PAD instructions (1AFF through ANDX) between each simulated instruction. Purging and padding introduce different timing to the instructions being executed. Options are available to eliminate both purging and padding. Test passes and conditions are repeatable. Conditions can be brought into a scope loop by typing LOOP or SSM. Random instructions are not changed by the repetition of a test pass.

RCT2 - Random Command Test

RCT2 is organized into 16 sections to test BDP instructions. Sections 0 through 6 test numeric instructions. Sections 7 through 12 test byte instructions. Sections 13 through 15 test immediate data instructions.

Section	BDP Instruction
0	Numeric Sum (70)
1	Numeric Difference (71)
2	Numeric Product (72)
3	Numeric Quotient (73)
4	Numeric Scale (E4) and Scale Rounded (E5)
5	Numeric Compare (74)
6	Numeric Move (75)
7	Byte Compare (77)
8	Byte Compare Collated (E9)
9	Byte Scan (F3)
10	Byte Translate (EB)
11	Byte Move (76)
12	Byte Edit (ED)
13	Immediate Data Move (F9)
14	Immediate Data Compare (FA)
15	Immediate Data Add (FB)

FCT1 - Fixed Operand Command Test

FCT1 is an inverted pyramid style of instruction test. Each test lists the instruction which should be checked before this test is run. The test automatically runs each instruction sequence. The test does not generate error messages other than expected and received results.

FCT2 - Fixed Operand Command Test

FCT2 is an inverted pyramid style of decision-point test. FCT2 tests the usage set for FCT3 and RCT1. If FCT2 runs correctly, further testing can be done at the instruction level. If FCT2 reports errors or does not run, there is no point in running any CPU-based test. Further diagnosis should be done using FCT1, FCT5, or microcode tests.

FCT3 - Fixed Operand Command Test

FCT3 is a usage set style of test. This test includes full operator control and detailed error messages. FCT3 tests all CPU-testable instructions using simple data patterns with emphasis on end cases.

FCT5 - Fixed Operand Command Test

FCT5 tests each instruction that the CPU cannot test fully. This test does not generate error messages other than expected and received results. FCT5 requires that FCT1 has run successfully.

FCT9 - Virtual Mode Instruction Level Test

FCT9 is organized into 13 sections to test virtual instructions.

Section	Description
0	Initializes FCT9.
1	Tests CRXj (660) instruction.
2	Tests CWXj (670) instruction.
3	Tests RXj (014) instruction in UEM (ECS mode).
4	Tests WXj (015) instruction in UEM (ECS mode).
5	Tests REC (block read ECS, 011) instruction in UEM (ECS mode).
6	Tests WEC (block write ECS, 012) instruction in UEM (ECS mode).
7	Tests error exits of CRXj and CWXj instructions.
8	Tests error exits of RXj and WXj instructions.
9	Tests error exits and half exits for block copy instructions in UEM (ECS mode). Full exits, where execution continues normally, are tested in sections 5 and 6.
10	Tests illegal instruction, address out of range, indefinite, and infinite error exits.
11	Tests RT (017) instruction.
12	Tests simulation of CMU instructions. Only interrupts and error exits are tested. (CT8 tests CMU instructions.)

EXCH - Exchange Test

EXCH is organized in 19 sections to test the exchange hardware.

Section	Description
0	Initializes virtual environment for sections 1 through 18.
1	Tests program swap mechanism used by CEJ/MEJ commands.
2	Tests PP exchange (2600) instruction and its addressing of CM.
3	Tests PP exchange (2600, 2610, 2620) instructions in CYBER 170 job and monitor mode.
4	Tests PP exchange (2600, 2610, 2620) instructions in executive state job mode.
5	Tests system's exchange interrupt response to PP exchange (2600, 2610, 2620) instructions while in executive state job mode.
6	Tests system's exchange interrupt response to PP exchange (2600, 2610, 2620) instructions while in executive state monitor mode.
7	Tests system's exchange interrupt response to PP exchange (2600) instruction by ensuring that B0 of the CYBER 170 exchange package is zero. (Register B0 is always zero in CYBER 170 environment.)
8	CP is placed in CYBER 170 mode and executes an X register shift sequence. Simultaneously, one to four PPs execute 26xx exchanges or 60- and 64-bit block writes. This section checks that these asynchronous operations produce no conflicts and complete successfully.
9	Similar to section 8 except another PP is continuously stopping and starting instruction execution. This test ensures that a process can be stopped and saved, that various registers can be read and written, and the process can then be reloaded and restarted successfully.
10	Similar to section 8 except a PP executes an INPN (102601) instruction instead of a 2600 instruction. This test ensures that external interrupts are handled successfully during 2600 exchanges.
11	Similar to section 8 except executive state CP code causes system and process interval timer (SIT and PIT) exchange and trap interrupts to occur at fast rates. This test verifies SIT and PIT traps and ensures that failures due to conflicts do not occur.
12	Tests illegal CYBER 170 instruction error exits.
13	Tests address out of range (AOR) error exits.

Section	Description
14	Tests infinite error exit conditions on floating point add, subtract, multiply, and divide instructions.
15	Tests indefinite error exit conditions on floating point add, subtract, multiply, and divide instructions.
16	Similar to section 2 except CM addresses are controlled by selectable parameters instead of a fixed table of addresses. This test permits a 2600 exchange instruction to be checked at any CM address above where this test resides.
17	Tests IOU's OS bounds register using PP 2610 exchange request instructions.
18	Tests a state switching mechanism which employs CYBER 170 X0 register sign bit. There are two conditions in which X0 sign bit is set and CEJ/MEJ (013) instruction is executed. When the CP is in 170 monitor mode, state should switch to executive state monitor mode. When the CP is in 170 job mode, no state switch should occur. However, a 170 exchange should occur and execution should commence in 170 monitor mode.

TRAP - Trap Test

TRAP is organized in 42 sections to test the monitor condition register (MCR), user condition register (UCR), and multiple interrupts.

Section	Description
0	Tests MCR bits. Performs various tests by setting MCR bits and checking the CP's response.
1	Tests UCR bits. Performs various tests by setting UCR bits and checking the CP's response.
2	Tests MCR bit 0. Generates an uncorrectable error interrupt. The CP causes this interrupt by writing to a CM cell that is defined as out of bounds by the CM bounds register.
3	Tests MCR bit 1 (reserved for future use).
4	Tests MCR bit 2 (tests short warning only if operator sets this section select bit.)
5	Tests MCR bit 3 - instruction specification error.
6	Tests MCR bit 4 - address specification error.
7	MCR bit 5 (exchange request not tested by TRAP).
8	Tests MCR bit 6 - access violation.
9	Tests MCR bit 7 - environment specification error.
10	Tests MCR bit 8 - external interrupt.
11	Tests MCR bit 9 - page table search.
12	Tests MCR bit 10 - system call.
13	Tests MCR bit 11 - system interval timer.
14	Tests MCR bit 12 - invalid segment/ring=0.
15	Tests MCR bit 13 - outward call/inward return.
16	Tests MCR bit 14 - soft error log.
17	Tests MCR bit 15 - trap exception.
18	Tests UCR bit 0 - privileged instruction fault.
19	Tests UCR bit 1 - unimplemented instruction.
20	Tests UCR bit 2 - free flag.
21	Tests UCR bit 3 - process interval timer.

Section	Description
22	Tests UCR bit 4 - inter-ring pop.
23	Tests UCR bit 5 - critical frame flag.
24	Tests UCR bit 6 - keypoint.
25	Tests UCR bit 7 - divide fault.
26	Tests UCR bit 8 - debug.
27	Tests UCR bit 9 - arithmetic overflow.
28	Tests UCR bit 10 - exponent overflow.
29	Tests UCR bit 11 - exponent underflow.
30	Tests UCR bit 12 - floating point loss of significance.
31	Tests UCR bit 13 - floating point indefinite.
32	Tests UCR bit 14 - arithmetic loss of significance.
33	Tests UCR bit 15 - invalid BDP data.
34	Tests CP's response to multiple interrupts.
35	Tests that no MCR bit is set in CM if corresponding mask bit is set when performing executive state exchange from monitor to job mode.
36	Reserved for future use.
37	Not used.
38	Not used.
39	Reserved for future use.
40	Not used.
41	Tests timer field in the keypoint buffer entry and the addressing and incrementing of the keypoint buffer pointer.

RFST - Random Fast/Slow Test

RFST generates a random set of instructions and operands each pass. On the first pass, the random set of instructions is executed and the results are saved. Then the instruction stream is executed again with the results saved. The results for both operations are compared. Any result difference causes an error. In the next step, one pad instruction is inserted between each instruction and the results are saved and compared as with the original non-padded result. This process repeats with the pad count incrementing to 16. This completes one pass. Each succeeding pass generates a new set of random instructions and operands.

DEBUG - Debug Test

DEBUG generates a random set of instructions and operands each pass. A simulated debug buffer is created (based on the debug code) to save the debug index and P counter for each instruction that causes a debug trap. The random instruction stream executes with debug disabled; all results are saved. Debug is then enabled and the random instructions are executed again. The results are saved and compared with the previous results. The actual debug buffer (created by the trap handler) is compared to the simulated buffer to ensure that debug occurred correctly. Each individual debug code is used with a combination of all codes (read, write, fetch, branch, call). After executing with each code and then the combination, one test pass is complete. Each succeeding pass generates a new set of random instructions and operands.

KYPT - Keypoint Test

KYPT tests the normal and abnormal operation of the system instruction keypoint. Sections 0 through 7 are the normal phase. That is, no interrupts associated with the instruction are expected. Sections 8 through 11 are the abnormal phase. Execution of the instruction causes an exchange interrupt to monitor mode. The abnormal phase tests the exception conditions associated with the instruction.

CACH - Cache Test

CACH tests the addressing and control sequences within the cache memory.

CP/CM Model Dependent Tests (ALLMD3)

ALLMD3 consists of the 15 model dependent tests described in the following paragraphs and listed below. ALLMD3B runs the same tests on CP-1 of a dual-CP system.

Test	Name
ACT3/P	Address Control (AC) Test
ANT3/P	Arithmetic and Logic Network (ALN) Test
BPT3/P	Business Data Processor (BDP) Test
CMT3/P	Central Memory (CM) Test
CST3/P	Control Store (CST) Basic Paths Test
CTT3/P	Common CST/Maintenance Access Control (MAC) Test
ICT3/P	Instruction Completion Control (ICC) and Instruction Control Pipeline (ICP) Test
IFT3/P	Instruction Fetch (IF) Test
LMT3/P	Local Memory (LM) Test
MAT3/P	Memory Array Identification Test
MCT3/P	MAC Test
MDT3/P	ALN Multiply/Divide Test
OIT3/P	Operand Issue (OPI) Test
PDT3/P	Processor Detected Malfunction and Associated Logic Test
SMT3/P	Segment Map (SM) Test

The ALLMD3 tests run in the following order.

1. CMT3/P
2. MCT3/P
3. CST3/P
4. IFT3/P
5. CTT3/P
6. OIT3/P
7. ACT3/P
8. LMT3/P
9. SMT3/P
10. ANT3/P
11. MDT3/P
12. BPT3/P
13. PDT3/P
14. ICT3/P
15. MAT3/P

Test descriptions include a reference to the level 2 diagram that depicts the hardware under test. Level 2 diagrams depict the following logic modules.

Diagram	Module
MAC 2.0	CSMC
IF 2.0, 2.1	IFIC
ICP 2.0	IFIC
ICC 2.0	IFIC
CST 2.0	CSMC
OPI 2.0	OPIA
OPI 2.1	OPIA, OPIB
OPI 2.2	OPIB
OPI 2.3	OPIA, OPIB
OPI 2.4, 2.5	OPSM
ALN 2.0-2.3	ALN
ALN 2.4-2.6	MD
AC 2.0-2.3	AC
BDP 2.0-2.3	BDP
SM 2.0	OPSM
LM 2.0	LMA, LMB
LM 2.1	LMA, LMB
CMC 2.0	CMCB
CMC 2.1	CMCA, CMCB
CM 2.0	CM Interface, Memory Modules

The following level 0 diagram relates ALLMD3 tests to the hardware under test.



ACT3/P - Address Control (AC) Test

Section	Description
Section 0	Verifies primary address path (AC 2.2, 2.3).
Subsection 0	Sends zeros and ones to the Untranslatable Pointer Register.
Section 1	Verifies primary address path (AC 2.2).
Subsection 0	Tests the A/B Operand (ADDRU) data path.
Section 2	Verifies primary address path (AC 2.2).
Subsection 0	Tests the Address Control Address Offset (OREG) data path and the Address Offset Select Mux (ADDR2).
Section 3	Tests addressing to Soft Control 1 memory (OUTDT1) (AC 2.1).
Subsection 0	Tests Soft Control 1 (OUTDT1) external address path.
Subsection 1	Tests Soft Control 1 (OUTDT1) internal address path.
Section 4	Does nothing. Kept as a spare.
Section 5	Tests the 32-bit Address Adder (AC 2.2).
Subsection 0	Tests intra-array (CG) logic.
Section 6	Tests the 32-bit Address Adder (AC 2.2).
Subsection 0	Tests signals between adjacent arrays.
Section 7	Tests the 32-bit Address Adder (AC 2.2).
Subsection 0	Tests remaining inter-array signals.
Section 8	Tests the 32-bit Address Adder (AC 2.2).
Subsection 0	Tests the Address Adder when in C170 mode.
Section 9	Tests the Load/Store Multiple Length (LSMPRE) Adder (AC 2.2).
Subsection 0	Tests LSMPRE input to the Address Offset Select Mux.
Subsection 1	Tests LSMPRE Adder, using valid combinations.
Subsection 2	Tests LSMPRE Adder, using invalid combinations.
Section 10	Tests the LM Byte Address Select Mux (ACAD) (AC 2.3).
Subsection 0	Tests the Mux input from the address adder.
Subsection 1	Tests the Mux input from the Address Control Stream address counter.

- Section 11 Tests error detection logic in the address calculation path (AC 2.2, 2.3).
- Subsection 0 Tests if parity errors can be forced and detected.
- Subsection 1 Tests parity error detection logic.
- Section 12 Tests address specification error and Address Control micrand parity (AC 2.0, 2.1).
- Subsection 0 Tests the address specification error sensing logic.
- Subsection 1 Tests the Address Control Micrand Register parity bits.
- Subsection 2 Tests the parity detection logic in the Address Control Micrand Register.
- Section 13 Tests C170 Mode Address Out of Range (AOR) (AC 2.3).
- Subsection 0 Verifies no AOR error occurs when the test address is equal to RAC but less than the RAC+FLC value.
- Subsection 1 Verifies AOR errors are generated when the test address is equal to or greater than FLC.
- Subsection 2 Verifies AOR errors are generated when the test address is less than RAC.
- Subsection 3 Verifies no AOR errors are generated when test address exceeds 18 bits before 8 times RAC is added to it.
- Section 14 Tests soft control addressing to the Soft Control 2 Memory (OUTDT2) (AC 2.1).
- Subsection 0 Tests OUTDT2 internal address entry.
- Subsection 1 Tests OUTDT2 external address entry.
- Section 15 Tests the A Stream data path (AC 2.0).
- Subsection 0 Tests the A Stream data path.
- Subsection 1 Tests the Right Byte Shifter data.
- Section 16 Tests byte positioning and selection within the A Stream data path (AC 2.0).
- Subsection 0 Tests the Right Byte Shifter shift count.
- Section 17 Tests mark bits generation logic (AC 2.1).
- Subsection 0 Tests mark lines and Address Adder Holding Register.
- Subsection 1 Tests Bit Right Shift Count register and the mark line parity logic.

- Section 18 Tests Final Address Control Stream (FAADS) byte number bits used to generate mark bits (AC 2.1).
- Subsection 0 Tests the FAADS input to the Mark Mask/Shift Count Mux.
- Section 19 Tests the byte load operation (AC 2.0).
- Subsection 0 Tests the A Stream byte load data path.
- Section 20 Tests byte instructions with word boundary (AC 2.0).
- Subsection 0 Tests byte load with Word Boundary Condition.
- Subsection 1 Tests byte store with Word Boundary Condition.
- Section 21 Tests Address Control Stream Address Counter and byte operations when run in sequence (AC 2.3).
- Subsection 0 Tests the Address Control Stream address counter.
- Subsection 1 Tests groups of byte instructions.
- Section 22 Tests Bit Load data path and control logic (AC 2.0).
- Subsection 0 Tests the Right Bit Shifter and the Final Load Bit entry to the A1/C1 Stream Buffer Register.
- Section 23 Tests Bit Store data path and control logic (AC 2.0).
- Subsection 0 Tests the Right Bit Shifter end around circuits and the Bit Store path.
- Section 24 Verifies the Test and Set Bit instruction (AC 2.0-2.3).
- Subsection 0 Tests the Test and Set Bit operation.
- Section 25 Tests bit instruction sequences (AC 2.0-2.3).
- Subsection 0 Tests combinations of bit operations.
- Section 26 Tests parity logic in the A Stream data path (AC 2.0).
- Subsection 0 Ensures that parity bits function and errors can be detected.
- Subsection 1 Tests the parity checkers and generators.

ANT3/P - Arithmetic and Logic Network (ALN) Test

Section 0	Checks basic Shift Mux and Shift Network (ALN 2.1).
Subsection 0	Tests Shift Mux response to Mux Code E.
Subsection 1	Tests Shift Network Rank 1 for shift counts of 1, 2, and 4 to bits 57 through 126.
Subsection 2	Tests Shift Network Rank 1 for shift counts of 1 through 7 to bits 57 through 126.
Subsection 3	Tests Shift Network Rank 2 for shift counts of 8, 16, and 32 for Rank 2 input bits 32 through 119.
Subsection 4	Tests Shift Network Rank 2 for shift counts of 8, 16, 24, 32, 40, 48, and 56 for Rank 2 input bits 8 through 119.
Subsection 5	Tests Shift Network Rank 1 for shift counts of 1 through 7 to bits 1 through 70.
Section 1	Tests Large Adder and does exhaustive test of shift network (ALN 2.1, 2.3).
Subsection 0	Tests data path from the shifter through the adder to the output Mux, forcing adder Mux to zero, and tests adder OR and ADD functions using a shift of 0 in the shifter.
Subsection 1	Tests shift count of 8 for the complete shifter using adder and shifter output paths.
Subsection 2	Tests shift count of 16 for the complete shifter using adder and shifter output paths.
Subsection 3	Tests shift count of 24 and sign extension for complete shifter using adder and shifter output paths.
Subsection 4	Tests shift count of 32 and sign extension for complete shifter using adder and shifter output paths.
Subsection 5	Tests shift count of 40 and sign extension for complete shifter using adder and shifter output.
Subsection 6	Tests shift count of 48 and sign extension for complete shifter using adder and shifter outputs.
Subsection 7	Tests shift count of 56 and sign extension for complete shifter using adder and shifter outputs.
Subsection 8	Tests shift count of 1 for the complete shifter using adder and shifter output paths.
Subsection 9	Tests shift count of 2 and sign extension for complete shifter using adder and shifter output paths.
Subsection 10	Tests shift count of 3 and sign extension for complete shifter using adder and shifter output paths.

- Subsection 11 Tests shift count of 4 and sign extension for complete shifter using adder and shifter output.
- Subsection 12 Tests shift count of 5 and sign extension for complete shifter using adder and shifter outputs.
- Subsection 13 Tests shift count of 6 and sign extension for complete shifter using adder and shifter outputs.
- Subsection 14 Tests shift count of 7, sign extension, and parity prediction using shifter and adder outputs.
- Section 2 Checks Shift Mux and Adder Mux (ALN 2.1, 2.3).
 - Subsection 0 Tests response of the Shift Mux and Adder Mux to complement code of complement RDSC in Shift Mux.
 - Subsection 1 Tests data path of RDSB through Exponent/Integer Mux and Adder Mux and Mux Code 0 control of the Adder Mux and Shift Mux.
 - Subsection 2 Tests Shift Mux and Adder Mux response to Mux Code 5.
- Section 3 Large Adder boolean and parity checks (ALN 2.3).
 - Subsection 0 Tests boolean functions in Large Adder bits 32 through 95.
 - Subsection 1 Tests boolean function control in Large Adder bits 32 through 95.
 - Subsection 2 Does final test of parity logic in Large Adder.
- Section 4 Checks Adder Mux and Shift Mux (ALN 2.1, 2.3).
 - Subsection 0 Tests Shift Mux response to Mux Code 1.
 - Subsection 1 Tests Adder Mux response to Mux Code 1.
 - Subsection 2 Tests Extend Zeros to Shift Network and Complement Code 1.
 - Subsection 3 Tests Shift Mux and Adder Mux response to Mux Code 2.
 - Subsection 4 Tests Shift Mux and Adder Mux response to Mux Code 3.
 - Subsection 5 Tests Shift Mux and Adder Mux response to Mux Code 4.
 - Subsection 6 Tests Shift Mux and Adder Mux response to Mux Code C.
 - Subsection 7 Tests Shift Mux and Adder Mux response to Mux Code D.

	Subsection 8	Tests Shift Mux and Adder Mux response to Mux Code 6.
	Subsection 9	Tests Shift Mux and Adder Mux response to Mux Code 7.
	Subsection 10	Tests Shift Mux and Adder Mux response to Mux Code F.
Section 5	Checks Large Adder and Carry Interchange (ALN 2.3).	
	Subsection 0	Tests Large Adder and Carry Interchange for proper handling of generates, enables, and satisfies.
	Subsection 1	Tests Carry Interchange for handling of enables.
	Subsection 2	Tests Carry Interchange for handling generates and satisfies End Around.
	Subsection 3	Does final test of Carry Interchange and End Around Carry.
Section 6	Checks Carry Code function for the Carry Interchange and Large Adder (ALN 2.3).	
	Subsection 0	Tests 18-bit Add Carry Code with sign extension.
	Subsection 1	Tests 60-bit Add Carry Code with sign extension.
	Subsection 2	Tests 32- and 64-bit twos Complement Adds, with automatic plus 1, Carry Codes.
	Subsection 3	Tests 32- and 64-bit twos Complement Adds, with conditional plus 1, Carry Codes.
Section 7	Checks overflow detection and reporting (ALN 2.0, 2.2).	
	Subsection 0	Tests 64-bit overflow detection and reporting.
	Subsection 1	Tests 32-bit overflow detection and reporting.
	Subsection 2	Tests 97-bit overflow detection and reporting.
Section 8	Checks Shift Count Generator (ALN 2.1).	
	Subsection 0	Tests Shift Count Generator Code 6 control.
	Subsection 1	Tests Shift Count Generator Codes 0, 1, and 2 control.
	Subsection 2	Tests Shift Count Generator Codes 3, 4, and 5 control.
Section 9	Checks Shift Count Generator outputs using micrand shift count inputs (ALN 2.1).	
	Subsection 0	Tests Shift Count Generator for shifts of 48, 32, and 16.
	Subsection 1	Tests Shift Count Generator for shifts of 8 and 4.
	Subsection 2	Tests Shift Count Generator for shifts of 2 and 1.

- Section 10 Checks latched shift count from Address Control and Shift Count Generator functions (AC 2.2, ALN 2.1).
- Subsection 0 Tests Address Control shift count data path through Address Control, and Shift Count Generator Codes 6 and 7.
 - Subsection 1 Tests Shift Count Generator Codes 0 and 2 with Address Control shift count.
 - Subsection 2 Tests Shift Count Generator Codes 1 and 3 with Address Control shift count.
 - Subsection 3 Tests Shift Count Generator Codes 4 and 5 with Address Control shift count.
 - Subsection 4 Tests Address Control Select of Address Control shift count bit 0.
- Section 11 Checks Right Shift 64 generation in Shift Count Generator and its use by the Shift Mux (ALN 2.1).
- Subsection 0 Tests Right Shift 64 generation and Mux Codes 4 and 5.
 - Subsection 1 Tests proper Right Shift 64 generation using Micrand Constant and Address Control shift count.
- Section 12 Checks shift fault logic (ALN 2.0).
- Subsection 0 Tests that Enable Shift Fault does not cause wrong select in output Mux.
 - Subsection 1 Tests shift fault detection and shifter output select on shift fault.
- Section 13 Checks Shift Count Generator using B and C operand paths (ALN 2.1).
- Subsection 0 Tests operation of Shift Count Generator Code B.
 - Subsection 1 Tests operation of Shift Count Generator Code 9.
 - Subsection 2 Tests operation of Shift Count Generator Code 8.
 - Subsection 3 Tests operation of Shift Count Generator Code A.
- Section 14 Does final check of Shift Count Generator output codes, and Mux code operations that use them (ALN 2.1, 2.3).
- Subsection 0 Tests C greater than B and Mux Code 8 operation.
 - Subsection 1 Tests Mux Code A operation.
 - Subsection 2 Tests Mux Code 6 response to Right Shift 64.
 - Subsection 3 Tests Mux Code 9 and SKG Code F.
 - Subsection 4 Tests SKG Code E and Adder Result Bit 47 Hold FF.

- Section 15 Checks Round Control in Adder Mux and Shift Mux (ALN 2.1, 2.3).
- Subsection 0 Tests Round operation in Shift Mux.
 - Subsection 1 Tests Round operation in Adder Mux.
- Section 16 Checks Complement Codes 1 and 3 (ALN 2.1, 2.3).
- Subsection 0 Tests Complement Code 1.
 - Subsection 1 Tests Complement Code 3 in Shift Mux.
 - Subsection 2 Tests Complement Code 3 in Adder Mux.
- Section 17 Checks the operation of Complement Codes 4, 5, 6, and 7 (ALN 2.0).
- Subsection 0 Tests Complement Code 4.
 - Subsection 1 Tests Complement Code 5.
 - Subsection 2 Tests Complement Code 6.
 - Subsection 3 Tests Complement Code 7.
- Section 18 Checks Normalize Encoder and associated logic (ALN 2.2).
- Subsection 0 Tests Normalize Encoder, Mux Code B, and more output data paths and controls.
 - Subsection 1 Tests XOR operation in Large Adder bits 0 through 31.
 - Subsection 2 Tests Significance Count Adjust Adder.
 - Subsection 3 Tests Normalize Control Code 4.
 - Subsection 4 Tests operation of micrand bits 24 and 25 and Adder Result Sign.
 - Subsection 5 Tests Adder Result Sign Selection in Carry Interchange.
- Section 19 Checks the Exponent Arithmetic Network and associated logic (ALN 2.2).
- Subsection 0 Tests Exponent Arithmetic Code 2 and Mux Code B.
 - Subsection 1 Tests Exponent Arithmetic Code 0.
 - Subsection 2 Tests Exponent Arithmetic Code 9 and A.
 - Subsection 3 Tests Exponent Arithmetic Code 7 and 8.
 - Subsection 4 Tests Exponent Arithmetic Codes 1, 3, and C.
 - Subsection 5 Tests Exponent Arithmetic Codes 5 and 6.
 - Subsection 6 Tests ability of normalize code to modify exponent arithmetic codes and to give arithmetic loss of significance.

- Section 20 Checks Force Zero out of ALN, nonstandard exponent detection and reporting, and force of nonstandard fixed values out of ALN (ALN 2.0).
 - Subsection 0 Tests force zeros in the Output Mux.
 - Subsection 1 Tests detection and reporting of 180 Exponent Overflow and 170 Infinite.
 - Subsection 2 Tests detection and reporting of 180 Exponent Underflow, 180 Indefinite and 170 Indefinite.
 - Subsection 3 Tests User Mask Register control of 180 exponent output.
 - Subsection 4 Tests detection of Floating Point loss of significance.
- Section 21 Checks Mark to Boolean and Enter Signs logic (ALN 2.0).
 - Subsection 0 Tests Mark to Boolean logic.
 - Subsection 1 Tests Signs Per J logic.
- Section 22 Checks compare code generation and reporting (ALN 2.0).
 - Subsection 0 Tests Integer compare.
 - Subsection 1 Tests 18-bit compare.
 - Subsection 2 Tests Floating Point compare.
- Section 23 Checks endcase exponent detection and reporting, User Mask Register and traps on ALN status (ALN 2.0).
 - Subsection 0 Tests user masks and traps.
 - Subsection 1 Tests 180 Subtract Endcase logic.
 - Subsection 2 Tests 180 Add Endcase logic.
 - Subsection 3 Tests Endcase Intermediate Cycle logic.
 - Subsection 4 Tests 180 Multiply Endcase logic.
- Section 24 Checks 170 Floating Point endcase detection, reporting and output (ALN 2.0).
 - Subsection 0 Tests 170 Floating Point add endcase.
 - Subsection 1 Tests 170 Floating Point subtract endcase.
 - Subsection 2 Tests 170 Floating Point multiply endcase.
 - Subsection 3 Tests Detect 170 Integer multiply.
 - Subsection 4 Tests 170 Floating Point divide endcase.

- Section 25 Checks 180 Floating Point divide endcase and block of Register File write on divide fault (ALN 2.0).
- Subsection 0 Tests 180 Floating Point divide endcase and divide fault logic.
- Section 26 Checks 170 Shift fault logic and special control from micrand bits 38, 62, and 63 (ALN 2.0).
- Subsection 0 Tests 170 nominal shift fault detection logic.
- Subsection 1 Tests micrand bits 62 and 38 use of zero hold logic.
- Subsection 2 Tests Double Precision loss of significance logic and remaining Zero Tests outputs from adder.
- Subsection 3 Tests micrand bit 38 block of force zeros output on detection of nonstandard input.
- Subsection 4 Tests ability of micrand bit 63 to force zero output.
- Subsection 5 Tests Force Copy C when micrand bit 38 is set and 170 Indefinite or Infinite is seen on input.
- Subsection 6 Tests remaining logic for detection of Arithmetic Overflow.
- Section 27 Checks branch logic in ALN (ALN 2.0).
- Subsection 0 Tests copy of ALN branch flip flop to compare code output.
- Subsection 1 Tests branch on 180, B equal to C, B not equal to C, B greater than C and B greater than or equal to C.
- Subsection 2 Tests branch on 170, B equal to C, B not equal to C, B less than C, B greater than or equal to C.
- Subsection 3 Tests 180 exception branch.
- Subsection 4 Tests 170 endcase branch, in range, not in range, definite, indefinite.
- Subsection 5 Tests 180 branch on segments not equal.
- Subsection 6 Tests block of branch on floating compare and branch when an input operand is indefinite.

- Section 28 Checks ALN instruction specification error, parity and carry error detectors and parity generators (ALN 2.0-2.3).
- Subsection 0 Tests instruction specification error.
 - Subsection 1 Tests carry error reporting using PTM bit 17.
 - Subsection 2 Tests parity error reporting from Large Adder.
 - Subsection 3 Tests parity error detection and reporting on ALN micrand field.
 - Subsection 4 Tests parity checkers for ALN micrand field.
 - Subsection 5 Tests Address Control shift count parity error reporting in ALN and Address Control using PTM bit 2.
 - Subsection 6 Tests Address Control shift count parity checkers and bits 0 through 5 generation.
 - Subsection 7 Tests exponent parity generation.

BPT3/P - Business Data Processor (BDP) Test

- Section 0 Tests Instruction Specification Error RAM (BDP 2.0, 2.3).
 - Subsection 0 Tests the generating of an Instruction Specification error bit.
 - Subsection 1 Tests the addressing of the Instruction Specification error RAM and the Rank 32 BDP Descr Type Field lines.
- Section 1 Tests Instruction Specification length error (BDP 2.0).
 - Subsection 0 Tests for Instruction Specification error for length error with the Descr Length Field lines.
- Section 2 Tests Basic data path (BDP 2.0, 2.1).
 - Subsection 0 Tests the basic data path (A and B Stream data lines to the BDP converted binary lines) along with BDP Cond Bits 2 and 3.
 - Subsection 1 Tests the address lines to the Conversion-to Binary/Decimal (Conv-to-Bin/Dec) RAM.
- Section 3 Tests Conv-to-Bin/Dec RAM data holding capabilities (BDP 2.3).
 - Subsection 0 Tests the addressing of the Conv-to-Bin/Dec RAM with an incrementing pattern.
 - Subsection 1 Tests further the addressing of the Conv-to-Bin/Dec RAM with a decrementing pattern.
- Section 4 Tests Address Control and BDP length counter (AC 2.2, BDP 2.0).
 - Subsection 0 Tests the A Stream of Address Control for a zero length check at the correct time.
 - Subsection 1 Tests the length counter in BDP for up to 9 bytes.
- Section 5 Tests Byte decode of A Stream in Address Control (AC 2.0).
 - Subsection 0 Tests the A Stream byte decode in Address Control while referencing the register file.
 - Subsection 1 Tests the A Stream byte decode in Address Control while referencing central memory.
- Section 6 Tests Word boundary and length counter of A Stream in Address Control (AC 2.0).
 - Subsection 0 Tests the A Stream length counter in Address Control for bytes within the same CM word.
 - Subsection 1 Tests the A Stream of Address Control for crossing of word boundaries.

- Section 7 Tests right-to-left sequence in A Stream of Address Control (AC 2.0).
- Subsection 0 Tests the A Stream length counter in Address Control for a right-to-left sequence.
 - Subsection 1 Tests the A Stream of Address Control for crossing word boundaries in a right-to-left sequence.
- Section 8 Tests C Stream of Address Control and the C(5) data bits of BDP (AC 2.0, BDP 2.3).
- Subsection 0 Tests the C(5) data bit lines to the C Stream of Address Control.
 - Subsection 1 Tests the byte decode on the C Stream of Address Control without crossing word boundaries.
- Section 9 Tests byte control and length counter in Address Control C Stream (AC 2.0).
- Subsection 0 Tests the length counter and the C(5) data bit register in Address Control and the AK length-equal-to-zero logic in BDP.
 - Subsection 1 Tests the length counter and byte control for the C Stream of Address Control in a right-to-left sequence.
- Section 10 Tests BDP Buffer RAM length counter (BDP 2.1).
- Subsection 0 Tests the length counter bits in BDP for the BDP Buffer RAM.
 - Subsection 1 Tests the length counter in the A Stream of Address Control for up to 3F₁₆ bytes for left-to-right and right-to-left.
- Section 11 Tests BDP Buffer RAM data (BDP 2.1).
- Subsection 0 Tests the BDP Buffer RAM for holding data correctly.
 - Subsection 1 Tests the A Stream of Address Control for crossing of word boundaries with 8 through 16 bytes.
- Section 12 Tests BDP Buffer RAM addressing (BDP 2.1).
- Subsection 0 Tests the A Stream of Address Control for crossing word boundaries with 8 through 16 bytes, right to left.
 - Subsection 1 Tests the addressing of the BDP Buffer RAM.
 - Subsection 2 Further tests the data holding capabilities of the BDP Buffer RAM.

- Section 13 Tests word boundary in C Stream of Address Control (AC 2.0).
- Subsection 0 Tests the C Stream of Address Control further for word boundary conditions.
 - Subsection 1 Tests the C Stream of Address Control further for word boundary conditions in a right-to-left sequence.
- Section 14 Tests Translate Encode RAM (BDP 2.3).
- Subsection 0 Tests the referencing of two consecutive register files by the A Stream of Address Control.
 - Subsection 1 Tests the Translate Encode RAM.
- Section 15 Tests B Stream data path (BDP 2.0).
- Subsection 0 Tests the B Stream data path to the BDP input Stream.
 - Subsection 1 Tests the B Stream length counter in Address Control for bytes in the same CM word.
- Section 16 Tests B Stream word decode in Address Control (AC 2.1).
- Subsection 0 Tests the B Stream word decode in Address Control while crossing word boundaries.
 - Subsection 1 Tests the B Stream word decode in Address Control while crossing word boundaries in a right-to-left sequence.
- Section 17 Tests B Stream length counter and A Stream addressing (AC 2.0, 2.1).
- Subsection 0 Tests the B Stream length counter in Address Control.
 - Subsection 1 Tests the decrementing of large addresses in the A Stream of Address Control, right-to-left sequence.
- Section 18 Tests Large addresses in B Stream of Address Control (AC 2.1).
- Subsection 0 Tests the incrementing of large addresses in the B Stream of Address Control.
 - Subsection 1 Tests the decrementing of large addresses in the B Stream of Address Control, right-to-left sequence.
- Section 19 Tests Addressing of the A and B Stream Decode RAMs (BDP 2.0).
- Subsection 0 Tests the addressing of the A and B Stream Decode RAMs in the BDP and the passing of the Translated EBCDIC bits from the RAM.

- Section 20 Tests Decimal/Binary (Dec/Bin) ALUs and Compares of Equal or Greater (BDP 2.3).
- Subsection 0 Tests the compare logic for an equal data function check.
 - Subsection 1 Tests the compare logic for a greater than function check.
- Section 21 Tests X0 and X1 Result Bits and compare for Less Than (BDP 2.1).
- Subsection 0 Tests the compare logic for a Less Than function check.
 - Subsection 1 Tests the RF10 (X0) Result Bits for correct transmitting.
 - Subsection 2 Tests the RF11 (X1) lines for a decimal compare operation.
- Section 22 Tests A and B Stream Exhausted signals plus fill (BDP 2.0).
- Subsection 0 Tests the A Stream Exhausted and B Stream Exhausted signals plus fill operation.
- Section 23 Tests BDP addition and subtraction logic (BDP 2.1).
- Subsection 0 Tests the addition logic in the BDP input stream.
 - Subsection 1 Tests the subtract logic in the BDP input stream.
- Section 24 Tests Form Combined Sign and ASCII Bias (BDP 2.1).
- Subsection 0 Tests the Form Combined Sign logic and the ASCII Bias logic in BDP.
 - Subsection 1 Tests the recomplementing logic in the BDP output stream.
- Section 25 Tests Slack Digit logic in BDP (BDP 2.1).
- Subsection 0 Tests the Slack Digit logic in BDP and the B Data signal.
- Section 26 Tests Immediate and Immediate One-shot logic (BDP 2.0).
- Subsection 0 Tests the Immediate and Immediate One-shot logic in BDP.
- Section 27 Tests Scale Left, Scale Right, and Rounding logic (BDP 2.0).
- Subsection 0 Tests the Scale Left logic in BDP.
 - Subsection 1 Tests the Scale Right logic and the Rounding logic in BDP.
 - Subsection 2 Checks the detection of Decimal Loss of Significance on a Scale Left operation.

- Section 28 Tests RF A RAM and Scan Hit Control (BDP 2.2).
- Subsection 0 Tests the RF A RAM for data and addressing capabilities.
 - Subsection 1 Tests the absence of a Scan Hit indication during a byte scan.
- Section 29 Tests RF B bit decoding and Scan Hit (BDP 2.2).
- Subsection 0 Tests that a Scan Hit can be generated.
 - Subsection 1 Tests for correct bit decoding in the RF B RAM.
- Section 30 Tests RF B data and sequence bits (BDP 2.2).
- Subsection 0 Tests the X0 Result bits for all of the sequence bits being transmitted.
 - Subsection 1 Tests the RF B RAM for proper data and addressing capabilities.
- Section 31 Tests Converter Decimal data path (BDP 2.3).
- Subsection 0 Tests the basic Converter Decimal data path in BDP.
 - Subsection 1 Tests the lower 2 ALUs in BDP Conv-to-Dec adders.
- Section 32 Tests Conv-to-Dec/Bin RAM address lines (BDP 2.3).
- Subsection 0 Tests bits 2^8 and 2^9 through the Conv-to-Dec Adders in BDP.
 - Subsection 1 Tests the address lines for the Conv-to-Dec/Bin RAM in BDP.
- Section 33 Tests Converter Multiply by 256 RAM and Conv-to-Dec Adders in convert logic (BDP 2.3).
- Subsection 0 Tests the address lines of the Converter Multiply by 256 RAM (times 256 RAM).
 - Subsection 1 Tests bits 2^8 to 2^{17} through the BDP convert logic.
- Section 34 Tests Converter Results RAM and Carry in Converter Decimal Adders (BDP 2.3).
- Subsection 0 Tests the carry operation in the converter logic.
 - Subsection 1 Tests the ability of the Converter Results RAM in the converter logic to hold data and be addressed correctly.
 - Subsection 2 Tests the moving of all data types from A Stream to all data types on C Stream, and check DLOS status.
 - Subsection 3 Tests DLOS status generated with various data types and length counts.
 - Subsection 4 Checks the A and B Stream Active signals in BDP.

- Section 35 Tests Pass data with the edit logic (BDP 2.2).
- Subsection 0 Tests the passing of data through BDP with an edit operation.
 - Subsection 1 Tests MOPO for translating data correctly in BDP.
- Section 36 Tests Edit Mask and the Symbol Mask RAM (BDP 2.2).
- Subsection 0 Tests the movement of data from the Edit Mask to the C Stream of Address Control.
 - Subsection 1 Tests the loading and addressing of the Symbol Mask (SM) RAM.
- Section 37 Tests Special Character Table RAM in edit logic (BDP 2.2).
- Subsection 0 Tests the loading and holding of data in the Special Character Table (SCT) RAM of BDP.
 - Subsection 1 Tests the addressing of the SCT RAM.
 - Subsection 2 Tests edit invalid data status detection.
- Section 38 Tests Generating and reporting of BDP parity errors (BDP 2.3).
- Subsection 0 Tests the Scale Counter parity detection.
 - Subsection 1 Tests the RF A Data parity detection + PTM(3).
 - Subsection 2 Tests the edit parity detection + PTM(4).
 - Subsection 3 Tests the sign digit and EBCDIC data parity detection.
 - Subsection 4 Tests the converter logic parity detection.
 - Subsection 5 Tests the altering of the Edit Mask by PTM(5).
 - Subsection 6 Tests the BDP micrand parity detection.
 - Subsection 7 Tests the Address Control B Stream data parity detection.
 - Subsection 8 Tests the A and B Stream descriptor lengths parity detection.
 - Subsection 9 Tests the BDP Convert-to-Binary lines to ALN unit parity detection.
 - Subsection 10 Tests the SVA latches in Address Control parity detection.
- Section 39 Tests Page table hit/miss on virtual BDP operation (ICP 2.0).
- Subsection 0 Tests proper latching in UTP register on hit/miss.

CMT3/P - Central Memory (CM) Test

Section 0	Checks MCH/MAC communication (MAC 2.0).
Subsection 0	Tests basic maintenance channel (MCH) response to function.
Subsection 1	Tests MCH echo function.
Subsection 2	Tests MCH data path from IOU and back using echo function.
Subsection 3	Tests MAC control logic related to Control Word flags.
Subsection 4	Tests MAC control logic related to Control Bytes Loaded flag.
Subsection 5	Tests response of MAC logic to a clear errors function.
Section 1	Checks MAC writing and reading capability (MAC 2.0).
Subsection 0	Tests write of all directly accessible processor registers.
Subsection 1	Tests read of all processor registers.
Subsection 2	Tests write of all processor Soft Control memories.
Subsection 3	Tests read of all processor Soft Control memories.
Subsection 4	Tests write of all processor Register File locations.
Subsection 5	Tests read of all processor Register File locations.
Subsection 6	Tests write of all processor Control Store memory.
Subsection 7	Tests read of all processor Control Store memory.
Subsection 8	Tests clear of MAC write FF.
Subsection 9	Tests clear of MAC read FF.
Subsections 10 through 15	Tests clock.
Section 2	Tests MAC bus data path (MAC 2.0).
Subsection 0	Tests the MAC bus data path from the PFS Register to MCH using zero data.
Subsection 1	Tests the MAC bus data path within the MAC.
Subsection 2	Tests the MAC bus data path from Address Control Soft Control through the ALN Soft Control to the IF Decode RAM.
Subsection 3	Tests the MAC bus data path legs from Register File to BDP Port A and B, and from Address Control Soft Control 1 to BDP RAM 0 and RAM 1.

- Section 3 Tests PFS Register (MAC 2.0).
- Subsection 0 Tests the byte and board select signals sent to and used on the PFS Register, as well as related control logic on the MAC.
 - Subsection 1 Tests the data path from the MAC through the memory maintenance register logic back to the MAC.
 - Subsection 2 Tests the gating of data from the memory maintenance registers to the MAC.
 - Subsection 3 Tests the multiplexing of upper and lower register selections.
 - Subsection 4 Tests the memory maintenance register byte parity generators.
 - Subsection 5 Tests memory maintenance register selection.
 - Subsection 6 Reads and reports on the Options Installed Register.
- Section 4 Tests the memory functions and basic data handling (CMC 2.0, 2.1; CM 2.0).
- Subsection 0 Tests basic write/read sequence of memory functions.
 - Subsection 1 Tests port input buffer memories.
 - Subsection 2 Tests Read and Set Lock function; holds function data to zero.
- Section 5 Continues Test of basic memory functions (CMC 2.0, 2.1; CM 2.0).
- Subsection 0 Tests Read and Set Lock function; holds memory data to zero.
 - Subsection 1 Tests Read and Clear Lock function; holds function data equal F---F₁₆.
- Section 6 Continues Tests of basic memory functions (CMC 2.0, 2.1; CM 2.0).
- Subsection 0 Tests Read and Clear Lock function; holds memory data equal F---F₁₆.
- Section 7 Tests the SECDED logic (CMC 2.0).
- Subsection 0 Tests the ECC generator and read syndrome generator.
 - Subsection 1 Tests the partial write ECC generator.
- Section 8 Continues test of SECDED Logic (CMC 2.0).
- Subsection 0 Tests the SECDED error reporting and correction logic.

- Section 9 Tests the detection and logging of errors; forces and verifies errors (CMC 2.0).
- Subsection 0 Tests the logging of the syndrome register A0 (CEL).
 - Subsection 1 Tests the logging of address bits to register A0.
 - Subsection 2 Tests the setting of the unlogged bit in register A0.
- Section 10 Continues test of error logs (CMC 2.0).
- Subsection 0 Tests the logging of address bits to maintenance register A4 (UNCCEL1).
 - Subsection 1 Tests the logging of a bounds fault into maintenance register A4.
 - Subsection 2 Tests the logging of data out path parity errors in maintenance register A4.
- Section 11 Continues test of error logs (CMC 2.0).
- Subsection 0 Tests the detection and logging of function parity errors into maintenance register A4.
 - Subsection 1 Tests the detection and logging of port parity errors in maintenance register A4.
 - Subsection 2 Tests the detection and logging of port parity errors in the port.
 - Subsection 3 Verifies that data written with a parity error will be read back without parity error.
 - Subsection 4 Tests the partial write logic using CM data having single bit errors.
 - Subsection 5 Tests the partial write logic using CM data having multiple bit errors.
 - Subsection 6 Tests the memory Status Summary register (SSUM).
- Section 12 Continues test of error logs (CMC 2.0).
- Subsection 0 Tests the detection and logging of Tag PE into maintenance register A8 (UNCCEL2).
 - Subsection 1 Tests the detection and logging of read parity errors into maintenance registers A4 and A8.

- Section 13 Tests the bounds detect logic (CMC 2.1).
- Subsection 0 Tests address out-of-bounds detection for lower bounds. The test address is greater than the bounds address.
 - Subsection 1 Tests address out-of-bounds detection for lower bounds. The test address is equal to one half the bounds.
 - Subsection 2 Tests bounds detection for lower bounds. The test address equal to the bounds address.
 - Subsection 3 Tests the Lower Bounds Register using addresses equal to twice the bounds address.
- Section 14 Continues test of bounds detect logic (CMC 2.1).
- Subsection 0 Tests bounds detection for upper bounds. Ensures that a write cannot be performed out-of-bounds. Ensures that a read is not so encumbered.
 - Subsection 1 Tests address out-of-bounds for upper bounds. The test addresses will be greater than the bounds address.
- Section 15 Continues test of bounds detect logic (CMC 2.1).
- Subsection 0 Tests address out-of-bounds for upper bounds. The test addresses will be equal to the upper bounds address.
 - Subsection 1 Tests the bounds vector bit (enable bounds).
- Section 16 Tests the memory arrays and their support logic (CM 2.0).
- Subsection 0 Tests the data fan-in and Address Control of the fan-in using zero data. Single bit errors are ignored unless they appear to be address related.
 - Subsection 1 Tests the data fan-in and Address Control of the fan-in using ones data.
- Section 17 Continues test of memory array support logic (CM 2.0).
- Subsection 0 Tests the data fan-in and Address Control of the fan-in using data equal 5---516.
 - Subsection 1 Tests the data fan-in and Address Control of the fan-in using data equal A---A16.
- Section 18 Continues test of memory arrays and supporting logic (CM 2.0).
- Subsection 0 Tests memory addressing; writes unique pattern to selected subset of memory. Each memory array is referenced several times.
 - Subsection 1 Reads and verifies memory written in subsection 0.

- Section 19 Continues test of memory arrays and supporting logic (CM 2.0).
- Subsection 0 Tests memory addressing; same as section 18, except that data is complemented.
 - Subsection 1 Tests memory addressing; same as section 18, except that data is complemented.
- Section 20 Tests memory arrays (CM 2.0).
- Subsection 0 Not used.
 - Subsection 1 Tests the memory arrays. Data patterns 5---5₁₆ and A--A₁₆ are used.
- Section 21 Continues test of memory arrays (CM 2.0).
- Subsection 0 Tests the memory arrays and chip addressing. An address pattern is used.
- Section 22 Tests the memory arrays and chip addressing (CM 2.0).
- Subsection 0 Tests the memory arrays and chip addressing. An address complement pattern is used.
- Section 23 Tests the memory using a march pattern (CM 2.0).
- Subsection 0 Tests the memory using a march pattern. The march pattern is generated using a Read and Set Lock function.
- Section 24 Consists of general tests (CMC 2.0, 2.1).
- Subsection 0 Verifies that write portion of read, modify, write sequence is aborted if an uncorrected error is detected in the read portion of the sequence.
 - Subsection 1 Verifies that bit 39 of maintenance register 20₁₆ does in fact inhibit entry to the corrected error log.
 - Subsection 2 Verifies that the disable parity check bit of maintenance register 20₁₆ does function as specified.
 - Subsection 3 Test logic that prevents a write to memory when a bounds fault is detected.
 - Subsection 4 Tests the data byte parity checkers in non-SECDED mode.
 - Subsection 5 Tests the page zero relocation feature of memory.

Section 25 Tests Port Disable logic (CMC 2.0, 2.1).

Subsection 0 Verifies that the port can be disabled by setting the proper bit in maintenance register 20₁₆.

Subsection 1 Verifies that the other ports can be disabled without effecting the IOU port.

Section 26 Utility section.

Subsection 0 Not used.

Section 27 Utility section.

Subsection 0 Not used.

Section 28 Tests central memory addressing (CMC 2.1).

Subsection 0 Uses a limited number of address bits to verify that all of the address lines work properly. Not all addresses are referenced.

CST3/P - Control Store (CST) Basic Paths Test

- Section 0 Tests basic Control Store operations (CST 2.0).
 - Subsection 0 Tests the start and stop logic during Control Store Sweep.
 - Subsection 1 Tests the Control Store Breakpoint Comparator logic.
 - Subsection 2 Tests Control Store Step Control logic while sweeping.
 - Subsection 3 Tests the MSC Parity Error/Fatal Error logic.
- Section 1 Tests basic micrand execution by Control Store (CST 2.0).
 - Subsection 0 Performs initial test of online micrand execution.
 - Subsection 1 Performs second test of online micrand execution to ensure that Control Store Sweep is not always enabled.
 - Subsection 2 Tests MIS=1 translation logic and MIS=1 setting Halt flag.
- Section 2 Tests the Control Store branching logic (CST 2.0).
 - Subsection 0 Performs first test of the Control Store Branch Delta Adder and the adder's Parity Predictor logic.
 - Subsection 1 Performs second test of the Control Store Branch Delta Adder and the adder's Parity Predictor logic.
 - Subsection 2 Performs final test of the Control Store Branch Delta Adder and the adder's Parity Predictor logic.
 - Subsection 3 Tests the branch to BA micrand execution and the BA field data bits path through the Control Store Micrand Address Mux1.
- Section 3 Tests the loading and use of the Control Store Return Register (CST 2.0).
 - Subsection 0 Tests Control Store's Return Register logic when entering the Return Register with the current micrand address.
 - Subsection 1 Tests loading the Return Register with the current micrand address +1.

- Section 4 Tests basic operation of copying FU micrand data to the Register File (CST 2.0, OPI 2.1).
- Subsection 0 Tests the transfer of FU micrand data to the Register File.
 - Subsection 1 Tests the RDSa to RDSw OPI Minipipe and the OPI Register File addressing when writing Register File with Immediate FU micrand data.
 - Subsection 2 Tests that no valids are enabled into the Control Pipe when Control Store is offline, and also when MIS field is 1 (Block Valid and set Halt flag).
- Section 5 Tests basic operation of transferring data from the Register File, through the ALN unit and back to the Register File (OPI 2.1, ALN 2.3, 2.4, 2.6).
- Subsection 0 Tests the basic Register File select paths for C operand and B operand to ALN, through ALN, back to DAI Mux Register and to Register File.
 - Subsection 1 Tests the OPI RDS Field Select Mux (RDS_c leg) and the Register File Address Select Mux (literal address leg).
 - Subsection 2 Tests the OPI RDS Field Select Mux (RDS_b leg).
- Section 6 Tests the basic registers in the Segment Map Unit (SM 2.0).
- Subsection 0 Tests the data path from RDSa operand select to Segment Map's PVA Register, New P Register, Old P Register and back to OPI Live Register Read Mux, then to the OPI Operand Data Mux.
 - Subsection 1 Tests the parity checkers along the data path from RDSa operand select to Segment Map's PVA Register, New P Register, Old P Register and back to OPI Live Register Read Mux, then to the OPI Operand Data Mux, through ALN, DAI Mux/Register and to the Register File.
 - Subsection 2 Tests the parity error reporting from the parity checkers for Segment Map's PVA Register, New P Register, Seg Descriptor Mux bits 16 through 31 and Address Control A/C Stream ASID Register.

- Section 7** Tests basic processor read and write central memory operations.
- Subsection 0** Tests the RDSa data path from OPI to Address Control Recovery Address Register (AC 2.3), the Untranslatable Pointer Register (bits 32 through 63) (ICP 2.0), the OPI Live Register Read Mux (OPI 2.5), and finally OPI Operand Data Mux (OPI 2.3).
 - Subsection 1** Tests the basic read data path from central memory (CM 2.0) to the Register File (OPI 2.1).
 - Subsection 2** Tests the processor read memory address path to central memory (CM 2.0).
 - Subsection 3** Tests the RDSd select bits path through the OPI RDS Write Selector Mux (RDSw) (OPI 2.0) and partial test of RDSa literal data through OPI Immediate Operand Mux (OPI 2.1).
 - Subsection 4** Tests the word write data path from OPI C Operand Register (OPI 2.3) to CMC/CM.
- Section 8** Tests processor logic involved in segment descriptor fetching (SM 2.0).
- Subsection 0** Tests the Segment Map Segment Descriptor Input Register, Segment Map Segment Descriptor Mux Shortstop leg, and the Segment Map Segment Descriptor Mux parity checkers.
 - Subsection 1** Tests that the Segment Map Seg Descriptor Mux parity checkers report parity errors.
 - Subsection 2** Perform a basic test of the Segment Descriptor Fetch logic.
 - Subsection 3** Tests the Segment Map P Descriptor Save Register data holding capability.
- Section 9** Tests Control Store conditional branching (SM 2.0, CST 2.0).
- Subsection 0** Tests the Segment Map C170 Mode flag and UVMID flag as well as Control Store C170 Mode and UVMID conditional branching.
 - Subsection 1** Tests Control Store Segment Map P Descriptor Local and/or Global Privilege conditional branching.
 - Subsection 2** Tests Control Store conditional branching when P Ring Number Initial is equal to P Ring Number Final, and the Segment Map Old/New P Ring Comparator.
 - Subsection 3** Tests Control Store Conditional Branching when Halt flag is set and when Halt flag is clear.
 - Subsection 4** Tests the toggling of the C180 Monitor Mode flag and Control Store conditional branching on C180 Monitor Mode Condition.

- Subsection 5 Tests the DAI Condition Select Register and Control Store conditional branching for different DAI Condition Select Register bit settings.
- Subsection 6 Performs final test of Control Store conditional branching when Test Mode (DEC bit 33) is set and clear.
- Subsection 7 Initializes subsection 9 conditions.
- Subsection 8 Tests Control Store conditional branching when checking forced condition false.
- Subsection 9 Tests that Control Store conditional branching to BD equals 0 and condition selects of 0C through 0F and 1C through 1F will block the pipe valid signal.
- Subsection 10 Completes testing of the Control Store Special Condition Select (SBDEQZ) logic circuit.
- Section 10 Tests basic processor instruction fetch operation.
 - Subsection 0 Tests Instruction Fetch Initialization (IF 2.1) and Control Store R125 Invalid Trap logic (CST 2.0).
 - Subsection 1 Tests that Control Store Pipe Valid (CST 2.0) is blocked when performing exit with R125 not valid.
 - Subsection 2 Performs initial test of the Control Store Exit micrand address formation for C180 and C170 Modes (CST 2.0).
 - Subsection 3 Tests Instruction Fetch (IF) P Register (IF 2.1) to ICP P Registers (ICP 2.0) to OPI Live Register Read Mux (OPI 2.5) data paths for P value of 0.
 - Subsection 4 Tests the writing of IF P Register (IF 2.1) from the DAI Register (OPI 2.3) and completes the testing of the data path from IF P Register through the Pipe (ICP 2.0) to OPI Live Register Read Mux (OPI 2.5).
 - Subsection 5 Tests the instruction word data path from central memory to IF.
 - Subsection 6 Tests the IF address data path from IF to local memory.

- Section 11** Tests remaining Control Store logic involved with fetching virtual instructions (CST 2.0).
- Subsection 0** Tests the C170 Op Code data path from IF C170 Decode RAMs, through the IF Buffer Word Assembly, and through the Control Store R125 address formation logic to the Control Store Micrand Address Mux1.
 - Subsection 1** Tests C170 Op Code to Control Store micrand address formation for C170 store instructions with and without Purge Instruction Stack Flag set.
 - Subsection 2** Tests Control Store micrand address formation when executing an exit to an unimplemented C180 instruction.
 - Subsection 3** Tests Control Store micrand address formation when executing an exit to a nonexecutable instruction.
 - Subsection 4** Does nothing subsection. Can be used for later test expansion.
 - Subsection 5** Tests proper operation of Control Store logic when micrand's GME field is equal to 2, void all pipe ranks and initialize instruction fetch.
- Section 12** Tests basic microcode trap operation (ICC 2.0).
- Subsection 0** Performs initial test of the Monitor Condition Register (MCR) for data holding capability. Also tests writing, reading, and read/clear of MCR.
 - Subsection 1** Performs final test of the MCR data holding capability.
 - Subsection 2** Performs initial test of the User Condition Register (UCR) for data holding capability. Also tests writing, reading, and read/clear of UCR.
 - Subsection 3** Performs final test of the UCR data holding capability.
 - Subsection 4** Tests that Write Monitor Condition Mask Register and Write User Condition Mask Register micrands execute without hanging up.
 - Subsection 5** Tests ICP Dead Man Timer (ICP 2.0), ICC Monitor Condition Register bit 0, ICC Trap Valid signal and partially tests Control Store Trap logic.
 - Subsection 6** Completes testing of the Control Store Trap logic and partially tests the ICC Micro Trap Code formation.
 - Subsection 7** Tests the ICC logic to verify that the Trap Valid signal drops after causing a Micro Trap.

CTT3/P - Common CST/Maintenance Access Control (MAC) Test

- Section 0 Tests stop control (CST 2.0).
- Subsection 0 Tests that Control Store logic operates correctly when a Stop MCH function is received and conditional exit micrands are being executed.
- Subsection 1 Tests that Control Store logic operates correctly when a Stop MCH function is received and unconditional exit micrands are being executed.
- Section 1 Tests MAC/Control Store logic involved with microcode assisted read operations (MAC 2.0, CST 2.0).
- Subsection 0 Tests that a MAC microcode assisted read request to Control Store causes a Micro Trap to CST address 30₁₆ while conditional exit micrands are being executed.
- Subsection 1 Tests that a MAC microcode assisted read request to Control Store causes a Micro Trap to CST address 30₁₆ while Control Store is spinning on a Set Halt Flag micrand.
- Subsection 2 Tests the MAC reference ROM data path to Control Store Micrand Address Register and the Control Store Branch to CST address indexed by reference ROM micrand control logic.
- Subsection 3 Tests the MAC addressing of the MAC reference ROM RAM for all microcode assisted register numbers.
- Subsection 4 Tests that a complete MAC microcode assisted read operation executes correctly when the processor is executing conditional exits.
- Subsection 5 Tests that a complete MAC microcode assisted read operation executes correctly when the processor is online and halted. Also test MAC lockout logic in Control Store.
- Subsection 6 Tests that a microcode assisted read request will not be honored by Control Store while unconditional exit micrands are being executed.
- Subsection 7 Tests the Control Store data path from MSC Register bits 6 through 10 to bits 0 through 4 of Micrand Address MUX2 Select, Select Reference ROM Address leg.
- Subsection 8 Tests that MAC RF ROM can be used as an entry point to the other half of Control Store (extended or normal), with CAE = 5.

- Section 2 Tests MAC/Control Store logic involved with microcode assisted write operations (MAC 2.0, CST 2.0, ICC 2.0).
- Subsection 0 Tests MAC and Control Store logic involved with microcode assisted write operation.
 - Subsection 1 Completes the testing of MAC and Control Store microcode assisted write logic.
 - Subsection 2 Tests that the ICC logic properly handles reporting deadman timeouts which occur during MAC microcode assisted operations.
 - Subsection 3 Tests the ICC logic which prevents writing into MCR and UCR when they are nonzero unless the writing is done as a MAC microcode assisted write.
- Section 3 Tests MAC/Control Store logic involved with microcode reading and writing MAC resident registers (MAC 2.0, CST 2.0).
- Subsection 0 Tests Control Store conditional branching logic for MAC Busy condition and the ability of Control Store to set MAC Busy FF.
 - Subsection 1 Tests that a MCH read of a directly accessible Processor Register, via the Processor MAC, causes the MAC Busy FF to set and that the MAC Busy FF is cleared when the read operation is complete (8 bytes transferred).
 - Subsection 2 Tests the OPI Reference ROM Address Register and the data path from the reference ROM Address Register to MAC reference ROM.
 - Subsection 3 Tests the OPI and MAC logic involved in an IU Read MAC Resident Register operation.
 - Subsection 4 Completes testing of MAC Data MUX5 to Data MUX6 data path.
 - Subsection 5 Tests the OPI and MAC logic involved in an IU Write MAC Resident Register operation.
- Section 4 Tests processor debug related logic (CST 2.0).
- Subsection 0 Tests the data holding capabilities of the Debug Mask Live Register and its parity checker.
 - Subsection 1 Tests Debug Mask Parity Checker error reporting.
 - Subsection 2 Performs initial test of Debug Hit logic.
 - Subsection 3 Tests Debug Lockout logic.
 - Subsection 4 Tests the Control Store logic that blocks the setting of the exit FF and causes a microtrap to Control Store address 7FF₁₆ when a Conditional Exit micrand is encountered with the Debug Lockout FF set.

- Subsection 5 Tests that Control Store Debug Lockout FF is cleared by an exit micrand.
- Subsection 6 Tests that a Debug Hit with micrand's MIS field equal to 2 will inhibit the writing of a live register.
- Subsection 7 Tests that Debug Hits occur correctly for different combinations of the Debug Mask Register bits and debug profile bits.
- Subsection 8 Tests MAC microcode assist requests to Control Store when Control Store is performing debug conditional exits.
- Section 5 Tests Control Store branch address parity regeneration logic (CST 2.0).
 - Subsection 0 Completes testing of the Control Store branch address parity regeneration upper logic.
 - Subsection 1 Completes testing of the Control Store branch address parity regeneration lower logic.

ICT3/P - Instruction Complete Control (ICC) and Instruction Control Pipeline (ICP) Test

- Section 0 Tests Stream Mode logic in OPI (OPI 2.4, 2.5).
 - Subsection 0 Performs initial test of Stream Mode logic in OPI.
 - Subsection 1 Tests Load Control circuits for the Process Interval Timer (PIT) and STA live registers in Stream Mode.
 - Subsection 2 Tests the Stream Mode Mux and the remaining live register write enable logic for Stream Mode.
- Section 1 Performs initial test of interrupt evaluation logic (ICC 2.0).
 - Subsection 0 Tests that Point-of-No-Return (PONR) can be taken without taking erroneous interrupts.
 - Subsection 1 Performs initial test of transfer of condition registers.
 - Subsection 2 Tests the Before FF.
 - Subsection 3 Tests that no PONR signals are stuck active to enable unwanted interrupts from the MCR or UCR.
- Section 2 Tests interrupts from the Rank 60 MCR and UCR (ICC 2.0).
 - Subsection 0 Tests the MCR Unmasked and Not Trap Interrupt State and MCR With Mask Clear Halt signal generation from the Rank 60 MCR.
 - Subsection 1 Tests the generation of the MCR Exchange/Trap/Stack signal from the Rank 60 MCR.
 - Subsection 2 Tests generation of the Masked UCR Trap/Stack signal from the Rank 60 UCR.
 - Subsection 3 Tests generation of the Unmasked UCR Trap/Exchange/Halt Interrupt signal from the Rank 60 UCR.
 - Subsection 4 Tests Halt Interrupts from the Rank 60 MCR and UCR.
 - Subsection 5 Tests Exchange Interrupts from the Rank 60 MCR and UCR.
 - Subsection 6 Tests Trap Interrupts from the Rank 60 MCR and UCR.
- Section 3 Tests the Rank 50 MCR and UCR, Rank 50 and Rank 60 ECR, and interrupts from these registers (ICC 2.0).
 - Subsection 0 Tests interrupts from Rank 50 MCR bits 0, 3, and 4, and the transfer of those bits to Rank 60.
 - Subsection 1 Tests interrupts from Rank 50 MCR bits 6, 7, 9, 12 and 13, and the transfer of those bits to Rank 60.
 - Subsection 2 Tests Rank 50 MCR bit 5, and Exchange Request and Accept logic in OPI and in the IOU.

- Subsection 3 Tests interrupts from Rank 50 MCR bit 5, transfer of that bit to Rank 60, 170 Exchange Interrupts, and the Exchange Accept signal to the IOU.
 - Subsection 4 Tests External Interrupts from the IOU, and MCR bit 8.
 - Subsection 5 Tests interrupts from Rank 50 UCR bits 7, 9, 13, 14 and 15, and the transfer of those bits to Rank 60.
 - Subsection 6 Tests interrupts from the Rank 50 and Rank 60 ECR, and transfer from the Rank 50 to the Rank 60 ECR.
- Section 4 Tests Retry logic (ICC 2.0).
 - Subsection 0 Tests that PTM bit 8 can set Rank 50 MCR(0) via Tests Retry.
 - Subsection 1 Tests Retry Interrupt generation and Retry Count parity error checking.
 - Subsection 2 Tests Retry Count loading and decrement, and determination of Successful Retry.
 - Subsection 3 Tests the Shadow Memory Retry in both halves of CS.
 - Subsection 4 Tests control transfer to extended Control Store with VMID.
- Section 5 Performs final test of interrupt priority logic (ICC 2.0).
 - Subsection 0 Performs exhaustive test of the interrupt priority logic and microtrap code parity.
- Section 6 Tests Exchange Interrupt State and Trap Interrupt State (ICC 2.0).
 - Subsection 0 Tests the Exchange Interrupt State FF and the Exchange Interrupt FF.
 - Subsection 1 Tests remaining untested logic for setting and clearing the Trap Interrupt State FF.
 - Subsection 2 Tests setting of Rank 60 MCR bit 15 in Trap Interrupt State.
- Section 7 Tests Clear Pipe and Inhibit Write Logic (ICC 2.0).
 - Subsection 0 Tests Clear Pipe generation, and inhibit of Register File and Live Register writes in OPI.
 - Subsection 1 Tests Branch Not Taken signal from ALN through IF to ICC, generation of the Gated Clear Pipe signal, and that Gated Clear Pipe blocks clearing of the condition registers.

	Subsection 2	Tests Gated Clear Pipe fan out to ICP, and the Clear Pipe FF in ICP.
	Subsection 3	Tests generation of LM Write Abort, and its effect in central memory.
Section 8	Tests Unbranch in IF and Rank 50 P Register in ICP (ICP 2.0).	
	Subsection 0	Tests the P Register bits 32-63 data path through Rank 50, and the Interrupt signal from ICC to IF.
	Subsection 1	Tests the ICP Rank 50 input to the IF Branch Address Adder A Input Mux. The +4 input to the Branch Address Adder B Input Mux is also tested.
Section 9	Performs exhaustive test of operand conflict resolution logic in OPI (ICP 2.0).	
	Subsection 0	Tests the RDSA and RDSB Recirculate Data Paths.
	Subsection 1	Tests the Register File Shortstop data path and the Rank 40 and Rank 50 comparators in the minipipe.
	Subsection 2	Tests the Operand Shortstop data paths between the ALN, Address Control, and LM functional units, and the B and C Operand Registers.
	Subsection 3	Tests the Rank 33 comparator in the minipipe.
	Subsection 4	Tests the Reload data path.
	Subsection 5	Tests generation of the B Operand Conflict signal and associated logic.
Section 10	Performs final test of the logic which enables faults into the Rank 50 Condition Registers (ICP 2.0).	
	Subsection 0	Tests the logic which enables the loading of faults into the Rank 50 Condition Registers.
Section 11	Tests operation of LM Write Abort Hold logic and Disable the Escaped Micrand logic (ICP 2.0).	
	Subsection 0	Tests LM Write Abort Hold and A Stream Abort Enable.
	Subsection 1	Tests Disable the Escaped Micrand operation.
Section 12	Tests decrementing of System Interval Timer (SIT) and PIT registers (OPI 2.5).	
	Subsection 1	Tests the SIT and PIT for correct decrementing.

IFT3/P - Instruction Fetch (IF) Test

- Section 0 Tests Basic P path and parity (IF 2.1).
 - Subsection 0 Tests the Master Clear processor function.
 - Subsection 1 Tests Initialize of IF.
 - Subsection 2 Tests entry of New P from OPI.
 - Subsection 3 Tests P path parity error reporting.
- Section 1 Tests CM load to IF (IF 2.0).
 - Subsection 0 Tests initial CM load to IF.
- Section 2 Tests Instruction Assembly Mux (IF 2.0).
 - Subsection 0 Tests C180 instruction leg of Mux.
 - Subsection 1 Tests C170 even RAM input to Mux.
 - Subsection 2 Tests C170 odd RAM input to Mux.
 - Subsection 3 Tests C170 leg of non-opcode portion of Mux.
- Section 3 Tests parcel select multiplexors (IF 2.0).
 - Subsection 0 Tests C180 parcel select Mux.
 - Subsection 1 Tests C170 parcel select Mux.
- Section 4 Tests P register incrementer (IF 2.1).
 - Subsection 0 Tests the incrementer with +2.
 - Subsection 1 Tests the incrementer with +4.
- Section 5 Tests the Branch Control Logic (IF 2.0).
 - Subsection 0 Tests branch indexed using Instruction Mux bit 42.
 - Subsection 1 Tests branch control with various target addresses.
- Section 6 Tests branch address adder input multiplexors (IF 2.0).
 - Subsection 0 Instruction Buffer Rank 2 to Adder.
 - Subsection 1 C180 Q times 2 input to adder.
 - Subsection 2 C170 reference address input to adder.
 - Subsection 3 C170 K times 4 input to adder.
- Section 7 Tests branch address adder (IF 2.0).
 - Subsection 0 Tests branch address adder.

Section 8 Tests AOR (IF 2.0).

Subsection 0 Tests the C170 Address-out-of-Range (AOR) detection.

Subsection 1 Tests AOR by sweeping through all addresses up to the maximum RAC + FLC.

Section 9 Performs miscellaneous tests (IF 2.0, 2.1).

Subsection 0 Tests gating of the Parcel 3 Save Register.

Subsection 1 Tests parity checkers following Instruction Buffer ranks 2 and 12.

Subsection 2 Tests BDP input leg of the Instruction Mux.

Subsection 3 Tests BDP control using two descriptors.

Subsection 4 Tests the parcel request control logic.

Subsection 5 Tests the Instruction Buffer ranks 3, 10, and 11.

Subsection 6 Tests the Address Specified Error detect logic, C170 mode.

Subsection 7 Tests the Address Specified Error detect in C180 mode.

Subsection 8 Tests the IFPURG signal to instruction fetch.

LMT3/P - Local Memory (LM) Test

- Section 0 Tests RMA address path (LM 2.0).
 - Subsection 0 Tests page size mask.
 - Subsection 1 Tests stream mode tag bits and CMC tag to CMC path.
 - Subsection 2 Tests the CMC Free Running Counter.
 - Subsection 3 Tests CMC Refresh and Interrupt functions.
 - Subsection 4 Tests RMA Bank Select/CM Busy.
- Section 1 Tests parity circuits using RMA addresses (LM 2.0).
 - Subsection 0 Tests LMTAG/CMTAG parity.
 - Subsection 1 Tests CM fault responses (part 1).
 - Subsection 2 Tests CM fault responses (part 2).
 - Subsection 3 Tests Page Offset/PSM parity.
 - Subsection 4 Tests RMA parity generation logic.
 - Subsection 5 Tests RMA parity error signals.
- Section 2 Tests preliminary cache checks (LM 2.1).
 - Subsection 0 Tests ACADDR/IFADDR through AMUX to Cache Sets 0 and 1.
 - Subsection 1 Tests ACADDR/IFADDR through AMUX to Cache Sets 2 and 3.
- Section 3 Tests cache data RAMs data integrity (LM 2.1).
 - Subsection 0 Tests Set 0 data test.
 - Subsection 1 Tests Set 1 data test.
 - Subsection 2 Tests Set 2 data test (if available).
 - Subsection 3 Tests Set 3 data test (if available).
- Section 4 Tests cache tag RAMs data integrity (LM 2.1).
 - Subsection 0 Tests Set 0 tag RAMs.
 - Subsection 1 Tests Set 1 tag RAMs.
 - Subsection 2 Tests Set 2 tag RAMs (if available).
 - Subsection 3 Tests Set 3 tag RAMs (if available).

- Section 5 Tests cache tag compare network (LM 2.1).
- Subsection 0 Tests Set 0 comparator.
 - Subsection 1 Tests Set 1 comparator.
 - Subsection 2 Tests Set 2 comparator (if available).
 - Subsection 3 Tests Set 3 comparator (if available).
- Section 6 Tests cache addressing, external to RAM (LM 2.1).
- Subsection 0 Tests Set 0 external addressing.
 - Subsection 1 Tests Set 1 external addressing.
 - Subsection 2 Tests Set 2 external addressing (if available).
 - Subsection 3 Tests Set 3 external addressing (if available).
- Section 7 Tests cache RAM addressing, tag and data (LM 2.1).
- Subsection 0 Tests Set 0 RAM addressing.
 - Subsection 1 Tests Set 1 RAM addressing.
 - Subsection 2 Tests Set 2 RAM addressing (if available).
 - Subsection 3 Tests Set 3 RAM addressing (if available).
- Section 8 Tests Purge Cache All (LM 2.1).
- Subsection 0 Tests Set 0 Purge All.
 - Subsection 1 Tests Set 1 Purge All.
 - Subsection 2 Tests Set 2 Purge All (if available).
 - Subsection 3 Tests Set 3 Purge All (if available).
- Section 9 Tests Cache Usable signal from MAC (LM 2.1).
- Subsection 0 Tests Set 0 Cache Usable.
 - Subsection 1 Tests Set 1 Cache Usable.
 - Subsection 2 Tests Set 2 Cache Usable (if available).
 - Subsection 3 Tests Set 3 Cache Usable (if available).
- Section 10 Tests cache parity circuits (LM 2.1).
- Subsection 0 Tests Set 0 parity circuits.
 - Subsection 1 Tests Set 1 parity circuits.
 - Subsection 2 Tests Set 2 parity circuits (if available).
 - Subsection 3 Tests Set 3 parity circuits (if available).
 - Subsection 4 Tests cache write data parity checker.

- Section 11 Tests cache parity error signals (LM 2.1).
 - Subsection 0 Tests cache write data parity signals.
 - Subsection 1 Tests mark data parity signals.
 - Subsection 2 Tests Cache Address parity signals.
 - Subsection 3 Tests Cache Address Register (CAR) PE, and Tag-In PE signals.
 - Subsection 4 Tests CHC Status verification.
 - Subsection 5 Tests Cache multi-hit test.
 - Subsection 6 Tests Cache RAM parity signals (CRAMPE).
- Section 12 Tests Purge cache functions (LM 2.1).
 - Subsection 0 Tests Purge Cache Block (512 bytes).
 - Subsection 1 Tests Purge Cache by ASID.
 - Subsection 2 Tests Purge Cache by ASID using upper CAR address.
- Section 13 Tests Cache Allocate and LRU Network (LM 2.0, 2.1).
 - Subsection 0 Tests Cache Allocate by Set Not Valid.
 - Subsection 1 Tests Cache Status RAM (LRU code only) data test.
 - Subsection 2 Tests Cache LRU Update network.
 - Subsection 3 Tests Status RAM parity signals.
- Section 14 Tests Address Control A Stream Counter (AC 2.0).
 - Subsection 0 Tests Address Control A Stream Counter.
- Section 15 Tests Page Table Address/Length Registers (LM 2.0).
 - Subsection 0 Performs PTA/PTL test, Part 1.
 - Subsection 1 Performs PTA/PTL test, Part 2.
- Section 16 Tests Page Table Address to RMA Mux (LM 2.0).
 - Subsection 0 Performs initial PTA to RMA Mux, Part 1.
 - Subsection 1 Performs initial PTA to RMA Mux, Part 2.
- Section 17 Tests hash code logic network (LM 2.0).
 - Subsection 0 Tests the Hash Shifter.
 - Subsection 1 Tests the PTA Exclusive OR (EXCL OR) logic.

- Section 18 Performs RMA incrementer test (LM 2.0).
 - Subsection 0 Tests searches up to 32 entries.
 - Subsection 1 Tests completes the incrementer test.
- Section 19 Tests RMA Mux, Incrementer Logic Merge (LM 2.0).
 - Subsection 0 Tests RMA Mux, Adder Merge, Part 1.
 - Subsection 1 Tests RMA Mux, Adder Merge, Part 2.
- Section 20 Tests PTA/PTL parity circuits (LM 2.0).
 - Subsection 0 Tests PTA/PTL parity checkers.
 - Subsection 1 Tests PTA/PTL and INCC parity signals.
- Section 21 Tests Page Table hit comparator (LM 2.0).
 - Subsection 0 Tests Page Table hit comparator, Match Valid.
 - Subsection 1 Tests Page Table hit comparator, Match Not Valid.
- Section 22 Tests RMA Mux, Page Frame Address entry (LM 2.0).
 - Subsection 0 Tests RMA Mux, Page Frame Address entry, Part 1.
 - Subsection 1 Tests RMA Mux, Page Frame Address entry, Part 2.
- Section 23 Tests MAP PFA/PO merge input to Final Mux Register (LM 2.0).
 - Subsection 0 Tests PFA/PO merge to final RMA Mux, Sets 0 and 1.
 - Subsection 1 Tests PFA/PO merge to final RMA Mux, Set 2.
 - Subsection 2 Tests Page Table hit, Prevalidated.
- Section 24 Tests Page Map data integrity (LM 2.0).
 - Subsection 0 Tests Page Map data test, Zeros Pattern.
 - Subsection 1 Tests Page Map data test, Ones Pattern.
 - Subsection 2 Tests Page Map data test, Alternate Bits 1.
 - Subsection 3 Tests Page Map data test, Alternate Bits 2.
- Section 25 Tests Page Map addressing (LM 2.0).
 - Subsection 0 Tests Set 0 Page Map addressing.
 - Subsection 1 Tests Set 1 Page Map addressing.
 - Subsection 2 Tests Set 2 Page Map addressing.

- Section 26 Tests Purge Page Map All (LM 2.0).
 - Subsection 0 Tests Set 0 Purge Map All test.
 - Subsection 1 Tests Set 1 Purge Map All test.
 - Subsection 2 Tests Set 2 Purge Map All test.
- Section 27 Completes Map Purge test (LM 2.0).
 - Subsection 0 Tests Purge by ASID, Purge by Page.
- Section 28 Tests Page Map comparator logic (LM 2.0).
 - Subsection 0 Tests Set 0 Page Map comparator.
 - Subsection 1 Tests Set 1 Page Map comparator.
 - Subsection 2 Tests Set 2 Page Map comparator.
- Section 29 Tests Page Map status RAM and Allocate test (LM 2.0).
 - Subsection 0 Tests Page Map Allocate and LRU Update.
 - Subsection 1 Tests Page Map status RAM data and address test.
- Section 30 Tests Page Map parity logic (LM 2.0).
 - Subsection 0 Tests Page Map (SPID/PFA) parity circuits.
 - Subsection 1 Tests Page Map parity error signals (MPASPE).
 - Subsection 2 Tests Page Map parity error signal (MPPFPE).
- Section 31 Tests Page Table Search and basic block fill (LM 2.0).
 - Subsection 0 Tests Page Table Search, Even/Odd address test.
 - Subsection 1 Tests Block read address (WBKAB) test.
- Section 32 Tests CM to Cache Data Path and Tag File test (LM 2.1).
 - Subsection 0 Tests Tag File 0, II/SA Requests.
 - Subsection 1 Tests Tag File 0, II/IF Requests.
 - Subsection 2 Tests Tag File 1, II/SA Requests.
 - Subsection 3 Tests Tag File 1, II/IF Requests.
 - Subsection 4 Tests Tag File 2, II/SA Requests.
 - Subsection 5 Tests Tag File 2, II/IF Requests.
 - Subsection 6 Tests Tag File 3, II/SA Requests.
 - Subsection 7 Tests Tag File 3, II/IF Requests.

- Section 33 Tests Cache Hit Valid logic (LM 2.1).
- Subsection 0 Tests Cache Hit Valid, Sets 0 and 1.
 - Subsection 1 Tests Cache Hit Valid, Sets 2 and 3.
- Section 34 Tests Cache Hit Not Valid and Associated RAMs (LM 2.1).
- Subsection 0 Tests Set 0 Cache Hit Not Valid and RAM test.
 - Subsection 1 Tests Set 1 Cache Hit Not Valid and RAM test.
 - Subsection 2 Tests Set 2 Cache Hit Not Valid and RAM test.
 - Subsection 3 Tests Set 3 Cache Hit Not Valid and RAM test.
- Section 35 Tests CMC tag decoder Rank A/Rank B logic and data (LM 2.0).
- Subsection 0 Tests Rank A response network.
 - Subsection 1 Tests Rank B logic and data, Part 1.
 - Subsection 2 Tests Rank B logic and data, Part 2.
- Section 36 Tests FAKECM and fault responses (LM 2.0).
- Subsection 0 Tests FAKECM responses.
 - Subsection 1 Tests Page Table fault responses.
 - Subsection 2 Tests Page faults with double response and test operations.
 - Subsection 3 Tests Special INDEX/TEST situations
 - Subsection 4 Tests Unique situation of memory request lockout.
- Section 37 Tests CM Invalidate/Cache Bypass (LM 2.0, 2.1).
- Subsection 0 Tests CM Invalidate and Cache Purge Four-Word Block.
 - Subsection 1 Tests Cache Bypass.
 - Subsection 2 Tests CM Invalidate bits continued.
- Section 38 Tests Tag File, AMUX, Block Fill data parity circuits (LM 2.0, 2.1).
- Subsection 0 Tests Tag File parity signal verification (TFADPE,TAGFPE).
 - Subsection 1 Tests SELRD Status Code and Block Fill data parity signal (CHCMPE) verification.
 - Subsection 2 Tests Address Mux parity error code verification (AMUXPE).

- Section 39 Tests Cache Lookahead, Part 1 (LM 2.1).
- Subsection 0 Tests Cache Lookahead, NXTBA to AMUX.
 - Subsection 1 Tests Cache Lookahead, verify operation.
 - Subsection 2 Tests Cache Lookahead, NXTBA Incrementer.
- Section 40 Tests Cache Lookahead, Part 2. (LM 2.1)
- Subsection 0 Tests Set 0, Status RAM bit 2 (BKUSED).
 - Subsection 1 Tests Set 1, Status RAM bit 2 (BKUSED).
 - Subsection 2 Tests Set 2, Status RAM bit 2 (BKUSED).
 - Subsection 3 Tests Set 3, Status RAM bit 2 (BKUSED).
- Section 41 Tests Cache Lookahead, Part 3 (LM 2.1).
- Subsection 0 Tests Inhibit Page Fault after Lookahead.
 - Subsection 1 Tests Unconditional/Conditional Lookahead Select.
 - Subsection 2 Tests Memory Requests Outstanding, PTCT Counter.
- Section 42 Tests Page Table update (LM 2.0).
- Subsection 0 Tests Update used bit in Page Table.
 - Subsection 1 Tests RMA Decrement for Update Address.
 - Subsection 2 Tests Update Modify during a Map Miss Write.
 - Subsection 3 Tests Update Modify in Map from Page Table.
- Section 43 Tests Page Map status RAM, Modify Bit (LM 2.0).
- Subsection 0 Tests Modify Bit integrity, Map Set 0.
 - Subsection 1 Tests Modify Bit integrity, Map Set 1.
 - Subsection 2 Tests Modify Bit integrity, Map Set 2.
- Section 44 Tests Page Map status parity circuits (LM 2.0).
- Subsection 0 Tests Page Map status RAM parity logic.
 - Subsection 1 Tests Page Map status RAM parity signal.
- Section 45 Tests LMMIC function code parity logic (LM 2.0).
- Subsection 0 Tests LMMIC parity checker.
 - Subsection 1 Tests CNTLP parity error signals.

- Section 46 Tests the CAR Equal (FESE) comparator (LM 2.0).
- Subsection 0 Tests FESE comparator, Write/Read Delay, Compare Valid.
 - Subsection 1 Tests FESE comparator, Write/Read Delay, Compare Invalid.
 - Subsection 2 Tests FESE comparator, LRU Shortstop.
- Section 47 Performs Conflict testing, allocation delays (LM 2.0).
- Subsection 0 Tests Conflict testing, Wait Allocate.
- Section 48 Tests Cache/Page Map conflicts (LM 2.0).
- Subsection 0 Tests Cache to Map conflict (CHTMP).
 - Subsection 1 Tests Read access and read/write conflict.
 - Subsection 2 Tests Cache allocation after Word Not Valid Hit.
 - Subsection 3 Tests Page Table update conflicts.
- Section 49 Tests Invalidate conflicts (LM 2.0).
- Subsection 0 Tests Invalidate conflict, Write/Cache Hit.
 - Subsection 1 Tests Invalidate conflict, Page Table Update.
 - Subsection 2 Tests Invalidate conflict, Cache Lookahead.
 - Subsection 3 Tests Invalidate conflict, Cache to Map.
 - Subsection 4 Tests Invalidate conflict, Wait Allocate.
 - Subsection 5 Tests Invalidate conflict, Cache Block Purge.
- Section 50 Tests Function Code bit +Func(1) (LM 2.0).
- Subsection 0 Tests Tests +Func(1) with CM-Exchange.
- Section 51 Performs additional test for +MHIT signal (LM 2.0).
- Subsection 0 Tests Tests random read/write/allocate.
 - Subsection 1 Performs final check of Page Map from Sub 0.

MAT3/P - Memory Array Identification Test (CM 2.0)

- Section 0 Tests data retention ability with suppression of Refresh-related faults.
 - Subsection 0 Tests data retention ability of each array module (or pair of modules) in turn, with suppression of Refresh-related faults.
- Section 1 Tests data retention ability without suppression of Refresh-related faults.
 - Subsection 0 Tests data retention ability of each array module (or pair of modules) in turn, without suppression of Refresh-related faults.
- Section 2 Tests address lines by testing for address uniqueness.
 - Subsection 0 Tests address lines on each module (or pair of modules) in turn, by testing for address uniqueness.
- Section 3 Tests memory array with multiple accesses to each address, with random data.
 - Subsection 0 Tests each array module (or pair of modules) in turn, with multiple accesses to each testable address, with random data.
- Section 4 Tests memory array with random data.
 - Subsection 0 Tests each array module (or pair of modules) in turn, with random data.
- Section 5 Tests all of testable memory with random data and random addresses.
 - Subsection 0 Tests all of testable memory with random data and random addresses.

MCT3/P - MAC Test

Section 0	Performs initial MCH/MAC communication check (MAC 2.0).
Subsection 0	Tests that a Master Clear function, Activate Channel and Deactivate Channel receive proper responses from the MAC logic.
Subsection 1	Tests that an Echo sequence operates correctly. Only one data pattern is used (FF ₁₆).
Subsection 2	Tests the basic MCH data path from the IOU to MAC and from MAC back to the IOU using the Echo function with various data patterns.
Subsection 3	Tests the MAC control logic specifically related to clearing the Control Word 1 FF and Control Word 2 FF.
Subsection 4	Tests the MAC control logic specifically related to clearing the Control Bytes Loaded FF.
Subsection 5	Tests that a Clear Errors function sent to MAC receives proper responses from MAC logic.
Section 1	Performs initial check of MAC writing and reading capability (MAC 2.0).
Subsection 0	Tests that MAC will write directly accessible process registers (Type 0) without hanging up.
Subsection 1	Tests that MAC will read all directly accessible process registers (Type 0) without hanging up.
Subsection 2	Tests that MAC will write all Soft Control memories (Types 3, 4, 5 and 6) without hanging up.
Subsection 3	Tests that MAC will read (Sweep) all Soft Control memories (Types 3, 4, 5 and 6) without hanging up.
Subsection 4	Tests that MAC will write all locations in the register file (Type 7) without hanging up.
Subsection 5	Tests that MAC will read all locations in the register file (Type 7) without hanging up.
Subsection 6	Tests that MAC will write all of Control Store memory (Type 1) without hanging up.
Subsection 7	Tests that MAC will read all of Control Store memory (Type 1) without hanging up.
Subsection 8	Tests the clearing of the write FF by the function signal.
Subsection 9	Tests the clearing of the read FF by the function signal.
Subsections 10 through 15	Clock tests.

- Section 2 Tests MAC data bus paths (MAC 2.0).
- Subsection 0 Tests the MAC data bus path from the PFS Register to MCH for passing zero data, and tests that certain PFS Register bits are clear.
 - Subsection 1 Tests the MAC data bus path within the MAC.
 - Subsection 2 Tests the MAC data bus path from Address Control Soft Control 2 through the ALN Soft Control to the IF Decode RAM.
 - Subsection 3 Tests the MAC bus data path legs from Register File to BDP Port A and B, and from Address Control Soft Control 1 to BDP RAM 0 and RAM 1.
- Section 3 Tests PFS Register boards (MAC 2.0).
- Subsection 0 Tests the byte and board select signals sent to and used on the PFS Register, as well as related control logic on the MAC.
 - Subsection 1 Tests the setting of all bits in the PFS Registers by writing the PFS Registers with byte data with bit 7 set to a one; causes all PFS Register bits to set.
 - Subsection 2 Tests the clearing of PFS Register bits by writing the PFS Registers with byte data with bit 7 clear. All bits cannot be guaranteed to clear at this point in the testing sequence; a partial test.
 - Subsection 3 Tests the PFS Board Select Translation logic, and the Error Log Board Select signals sent to the PFS Register.
 - Subsection 4 Tests that a Clear Errors Function clears the PFS Register bits; a partial test.
- Section 4 Tests MAC hardware error reporting (MAC 2.0).
- Subsection 0 Tests the MAC for reporting data errors on data received from the MCH.
 - Subsection 1 Tests the MAC for reporting channel errors when illegal opcodes and illegal type codes are sent to MAC.
 - Subsection 2 Tests the MAC parity checkers for reporting parity errors and checks that the MAC force bad parity circuits functions properly (PTM bit 18).
 - Subsection 3 Tests the parity error reporting on MAC bus data from PFS Register.
 - Subsection 4 Tests the parity error reporting from PFS Register.

Subsection 5	Tests the parity error reporting from PFS Register.
Subsection 6	Tests the parity error reporting from PFS Register.
Subsection 7	Tests the parity error reporting from PFS Register.
Subsection 8	Tests the parity error reporting from the MAC Reference ROM read data parity checker.
Subsection 9	Tests the MAC reporting of channel parity errors on Control Word 1, Control Word 2, and write data. Also ensures that these type parity errors are not reported as read data parity errors.
Section 5	Tests MAC hardware parity checkers (MAC 2.0).
Subsection 0	Tests the MAC parity checkers.
Subsection 1	Tests the parity checkers on the PFS Register and the MAC Mux 5.
Section 6	Tests MAC reference ROM memory (MAC 2.0).
NOTE	
Clock pulse width margins (PARAM1) are enabled by section 6 for the remaining test sections.	
Subsection 0	Tests the MAC reference ROM memory for holding data in all locations.
Subsection 1	Tests the MAC reference ROM read data parity checker.
Subsection 2	Tests the reference ROM memory addressing logic, both external and internal to the memory's RAM chips.
Section 7	Tests MAC address bus path (MAC 2.0).
Subsection 0	Tests MAC address bus path with various address patterns.
Section 8	Tests AC/ALN SCM error reporting and byte selects (MAC 2.0).
Subsection 0	Tests parity error reporting from Address Control Soft Control 2 and MAC Bus Byte Select path to Address Control Soft Control 2.
Subsection 1	Tests parity error reporting from Address Control Soft Control 1 and MAC Bus Byte Select path through Address Control Soft Control 2 to Address Control Soft Control 1.
Subsection 2	Tests parity error reporting from ALN Soft Control and MAC Bus Byte Select path through Address Control Soft Control 1 to ALN SCM.

- Section 9 Tests BDP RAM error reporting and byte selects (MAC 2.0).
- Subsection 0 Tests RAM parity error reporting from BDP Port A and MAC Bus Byte Select path through Address Control Soft Control 2 to the BDP Port A.
 - Subsection 1 Tests RAM parity error reporting from BDP Port B and MAC Bus Byte Select path through BDP Port A to BDP Port B.
 - Subsection 2 Tests RAM parity error reporting from BDP RAM 0, EBCDIC RAM, and the MAC Bus Byte Select path through BDP Port B to BDP RAM 0.
 - Subsection 3 Tests RAM parity error reporting from BDP RAM 0, Convert RAM.
 - Subsection 4 Tests RAM parity error reporting from BDP RAM 1, Spec Error RAM, and the MAC Bus Byte Select path through BDP RAM 0 to BDP RAM 1.
 - Subsection 5 Tests RAM parity error reporting from the BDP RAM 1, X256 RAM.
- Section 10 Tests IF Decode RAMs error reporting and byte selects (MAC 2.0).
- Subsection 0 Tests RAM parity error reporting from the IF C170 Decode RAMs.
 - Subsection 1 Tests RAM parity error reporting from the IF C180 Decode RAMs.
- Section 11 Tests MAC address bus error reporting (MAC 2.0).
- Subsection 0 Tests parity error reporting from the IF Instruction Assembly Register (bits 0 through 7 and 8 through 15) parity checkers, from the BDP Port A and Port B Stage 1 Register parity checkers, and from the BDP RAM 0 and RAM 1 Address Register parity checkers.
 - Subsection 1 Tests the parity error reporting from the BDP Port A and Port B Stage 2 Register (bits 0 through 7) parity checkers.
 - Subsection 2 Tests the parity error reporting from the BDP RAM 0 and 1 RAM Data Register (bits 0 through 7) parity checkers, EBCDIC and Spec Error RAMs.
 - Subsection 3 Tests the parity error reporting from the BDP RAM 0 and 1 RAM Data Registers (bits 0 through 7) parity checkers, Convert and X256 RAMs.

- Section 12 Tests IF C180 and C170 Decode RAM memories (IF 2.0).
- Subsection 0 Tests MAC address incrementer and parity predictor, and IF Instruction Assembly Register parity checkers for bits 0 through 7/64 and 8 through 15/65.
 - Subsection 1 Tests IF C180 Decode RAM memory chips with various data patterns, all locations.
 - Subsection 2 Tests IF C170 Decode RAM memory chips with various data patterns, all locations.
 - Subsection 3 Tests the IF C180 Decode RAM read data parity checkers.
 - Subsection 4 Tests the IF C170 Decode RAM read data parity checkers.
 - Subsection 5 Tests the IF C180 Decode RAM addressing logic.
 - Subsection 6 Tests the IF C170 Decode RAM addressing logic.
 - Subsection 7 Tests the addressing circuits internal to the IF C180 Decode RAM memory chips.
 - Subsection 8 Tests the addressing circuits internal to the IF C170 Decode RAM memory chips.
- Section 13 Tests Address Control Soft Control 1 RAM memories (AC 2.1).
- Subsection 0 Tests Address Control Soft Control 1 memory chips with various data patterns, all locations.
 - Subsection 1 Tests Address Control Soft Control 1 RAM read data parity checkers.
 - Subsection 2 Tests Address Control Soft Control 1 addressing logic.
 - Subsection 3 Tests the addressing circuits internal to the Address Control Soft Control 1 memory chips.
- Section 14 Tests Address Control Soft Control 2 RAM memories (AC 2.1).
- Subsection 0 Tests Address Control Soft Control 2 memory chips with various data patterns, all locations.
 - Subsection 1 Tests Address Control Soft Control 2 RAM read data parity checkers.
 - Subsection 2 Tests Address Control Soft Control 2 addressing logic.
 - Subsection 3 Tests the addressing circuits internal to the Address Control Soft Control 2 memory chips.

- Section 15 Tests ALN SC RAM memories (ALN 2.6).
- Subsection 0 Tests ALN SC memory chips with various data patterns, all locations.
 - Subsection 1 Tests ALN SC RAM read data parity checkers.
 - Subsection 2 Tests ALN SC addressing logic.
 - Subsection 3 Tests the addressing circuits internal to the ALN SC memory chips.
- Section 16 Tests BDP Port A memory (BDP 2.2).
- Subsection 0 Tests BDP Port A memory chips with various data patterns, all locations.
 - Subsection 1 Tests BDP Port A memory read data parity checkers.
 - Subsection 2 Tests BDP Port A addressing logic.
 - Subsection 3 Tests the addressing circuits internal to the BDP Port A memory chips.
- Section 17 Tests BDP Port B memory (BDP 2.2).
- Subsection 0 Tests BDP Port B memory chips with various data patterns, all locations.
 - Subsection 1 Tests BDP Port B memory read data parity checkers.
 - Subsection 2 Tests BDP Port B addressing logic.
 - Subsection 3 Tests the addressing circuits internal to the BDP Port B memory chips.
- Section 18 Tests BDP RAM 0 EBCDIC memory (BDP 2.3).
- Subsection 0 Tests BDP RAM 0 EBCDIC memory chips with various data patterns, all locations.
 - Subsection 1 Tests BDP RAM 0 EBCDIC memory read data parity checkers.
 - Subsection 2 Tests BDP RAM 0 EBCDIC memory addressing logic.
 - Subsection 3 Tests the addressing circuits internal to the BDP RAM 0 EBCDIC memory chips.
- Section 19 Tests BDP RAM 0 Convert memory (BDP 2.3).
- Subsection 0 Tests BDP RAM 0 Convert memory chips with various data patterns, all locations.
 - Subsection 1 Tests BDP RAM 0 Convert memory read data parity checkers.

	Subsection 2	Tests BDP RAM 0 Convert memory addressing logic.
	Subsection 3	Tests the addressing circuits internal to the BDP RAM 0 Convert memory chips.
Section 20	Tests BDP RAM 1 Spec Error memory (BDP 2.3).	
	Subsection 0	Tests BDP RAM 1 Spec Error memory chips with various data patterns, all locations.
	Subsection 1	Tests BDP RAM 1 Spec Error memory read data parity checkers.
	Subsection 2	Tests BDP RAM 1 Spec Error memory addressing logic.
	Subsection 3	Tests the addressing circuits internal to the BDP RAM 1 Spec Error memory chips.
Section 21	Tests BDP RAM 1 X256 memory (BDP 2.3).	
	Subsection 0	Tests BDP RAM 1 X256 memory chips with various data patterns, all locations.
	Subsection 1	Tests BDP RAM 1 X256 memory read data parity checkers.
	Subsection 2	Tests BDP RAM 1 X256 memory addressing logic.
	Subsection 3	Tests the addressing circuits internal to the BDP RAM 1 X256 memory chips.
Section 22	Tests Register File (OPI 2.1).	
	Subsection 0	Tests parity error reporting from the Register File read data parity checkers and the MAC Register File byte selection logic.
	Subsection 1	Tests the Register File with various data patterns, all locations, and the Control Store Disassembly Network byte selection logic.
	Subsection 2	Tests the Register File read data parity checkers and addressing logic external to the Register File memory chips.
	Subsection 3	Tests the addressing circuits both external and internal to the Register File memory chips.
Section 23	Tests Control Store Breakpoint and Micrand Address Registers (CST 2.0).	
	Subsection 0	Tests MAC capability to write and read the Control Store Breakpoint Register with various data patterns.
	Subsection 1	Tests the parity generator on the MAR/BKPT data path to MAC Mux2.

- Subsection 2 Tests MAC capability to write and read the Control Store Micrand Address Register with various data patterns, and test the Control Store Micrand address parity regeneration logic.
 - Subsection 3 Tests parity error reporting from the Control Store Micrand Address Register parity checker.
 - Subsection 4 Tests the Control Store Micrand Address Register parity checker.
- Section 24 Tests Control Store memory (CST 2.0).
 - Subsection 0 Tests parity error reporting from the Control Store memory data parity checkers and the MAC Control Store byte selection logic.
 - Subsection 1 Tests the Control Store memory with various data patterns, all locations; the Control Store Micrand Address Incrementer logic; and the MAC Control Store read data path.
 - Subsection 2 Tests the Control Store memory data parity checkers and partial test of the addressing logic.
 - Subsection 3 Tests the Control Store memory addressing logic both external and internal to the Control Store memory chips.
- Section 25 Completes test of MAC Byte Select logic (MAC 2.0).
 - Subsection 0 Completes testing of the MAC Byte Select signal formation for Type 4 Soft Control Memories (Address Control and ALN).
 - Subsection 1 Completes testing of the MAC Byte Count translation logic.
 - Subsection 2 Completes testing of the MAC Register File Byte Select Decoder logic.
- Section 26 Completes test of MAC Type Decode logic (MAC 2.0).
 - Subsection 0 Completes testing of the MAC Type Decode logic.
- Section 27 Completes test of MAC Go Decoder (MAC 2.0).
 - Subsection 0 Completes testing of the MAC Soft Control Go Decoder circuits involved with generation of the Go Soft Control memory signals.
 - Subsection 1 Completes testing of the MAC BDP Control Memory Go Decoder circuits involved with generation of the Go BDP memory signals.

- Section 28 Performs miscellaneous MAC logic testing (MAC 2.0).
- Subsection 0 Tests MAC Data Mux4 and complete the testing of MAC Data Mux5.
 - Subsection 1 Performs a partial test of MAC Data Mux1 and Data Mux2.
 - Subsection 2 Tests that a Master Clear function to processor MAC generates Soft Control Go signals to the Address Control and ALN Soft Control memories, and function signal clears MAC Address Incrementer.
- Section 29 Test first failure capture feature (MAC 2.0).
- Subsection 0 Test first failure capture feature of system by forcing clock errors.
 - Subsection 1 Restore system clock delays.

MDT3/P - ALN Multiply/Divide Test

- Section 0** Checks ALN Soft Control memory addressing and Minor Cycle Control Register (ALN 2.6).
- Subsection 0** Tests the Minor Cycle Control Register for parity status in Idle state, parity error detection and reporting, and Clock Enable controls from Soft Control memory.
 - Subsection 1** Tests Soft Control memory addressing from ALN micrand field and Minor Cycle clock.
 - Subsection 2** Tests Minor Cycle Control Register parity checkers and all bit paths into the register.
- Section 1** Checks of C Register entry controls and sign extension (ALN 2.4).
- Subsection 0** Tests C Register select of shifted data and sign extension from bit 0.
 - Subsection 1** Tests 32-bit sign extension in Divide Quotient Register and C Register entry from Divide Quotient Register.
 - Subsection 2** Tests C Sign Selection logic under 170/180 mode micrand control and its entry into the C Register.
 - Subsection 3** Tests Unsigned C Register entry from Major and Minor Cycle controls.
- Section 2** Basic checks of multiply logic (ALN 2.4, 2.5).
- Subsection 0** Tests that the multiply logic does not pick up bits when multiplying zero times zero and one times zero.
 - Subsection 1** Tests the following areas of the multiply logic: B Register, B Product network for 1x decodes and partial sum generation, Multiply Partial Summing network for partial sum generation, the Final Adder and Multiply/Divide Output Mux.
 - Subsection 2** Tests the following areas of the logic: A Product network for 1x decode and partial sum generation, and the Multiply Partial Summing network for partial sum generation.
 - Subsection 3** Tests B Product network for partial carry generation and the Multiply Partial Summing network for partial sum generation.
 - Subsection 4** Tests the A Product network for partial carry generation and the Multiply Partial Summing network for partial sum generation.
 - Subsection 5** Tests B Product network for partial carry generation from 1x decodes in C Register bits 69 through 71 and 67 through 69.

- Subsection 6 Tests A Product network for partial carry generation from 1x decodes in C Register bits 63 through 65 and 61 through 63.
- Subsection 7 Tests B Product network for partial carry generation from 1x decodes in C Register bits 71 through 73 and 69 through 71.
- Subsection 8 Tests A Product network for partial carry generation from 1x decodes in C Register bits 65 through 67 and 63 through 65.
- Subsection 9 Tests B Product network for partial carry and partial sum generation.
- Subsection 10 Tests A Product network for partial carry and partial sum generation.
- Subsection 11 Tests Multiply Partial Summing network for summing of an A Product network partial sum with a B Product network partial sum.
- Subsection 12 Tests Multiply Partial Summing network for summing of an A Product network partial sum with a B Product network partial carry.
- Subsection 13 Tests the Multiply Partial Summing network for the summing of a Partial Carry from the A Product with a Partial Sum from the B Product network.
- Subsection 14 Tests the Multiply Partial Summing network for Partial Carry 2 generation and the Multiply Final Adder for adding of Multiply Partial Carry bits.
- Subsection 15 Tests the Multiply Partial Summing network for generation of $N+2$ carry.
- Subsection 16 Tests the Multiply Partial Summing network for summing of a Multiply Partial Sum bit with a Net B Partial Carry bit.
- Subsection 17 Tests the Multiply Partial Summing network for summing of a Multiply Partial Carry bit with a Net B Partial Sum bit.
- Subsection 18 Tests 1x, -2x and Complement Correction decodes from C Register bits 65 through 73 to the B and A Product networks.
- Subsection 19 Tests 1x, -2x and Complement Correction decodes from C Register bits 65 through 73 to the B and A Product networks and the Upper Multiply Partial Summing network.
- Subsection 20 Tests 1x, -2x and Complement Correction decodes from C Register bits 61 through 67 to the A Product network.

Subsection 21	Tests the 1x, -2x and Complement Correction decodes from C Register bits 61 through 67 to the A Product network and the upper bits of the Multiply Partial Summing Network.
Subsection 22	Tests 2x decodes to the B Product network.
Subsection 23	Tests the 2x decodes to the B Product network and the upper bits of the Multiply Partial Summing network.
Subsection 24	Tests 2x decodes to the A Product network.
Subsection 25	Tests the 2x decodes to the A Product network and the upper bits of the Multiply Partial Summing network.
Subsection 26	Tests -1x decodes to the B Product network.
Subsection 27	Tests the -1x decodes to the B Product network and the upper bits of the Multiply Partial Summing network.
Subsection 28	Tests -1x decodes to the A Product network.
Subsection 29	Tests the -1x decodes to the A Product network and the upper bits of the Multiply Partial Summing network.
Subsection 30	Tests -1x decodes to the B Product network.
Subsection 31	Tests the -1x decodes to the B Product network and the upper bits of the Multiply Partial Summing network.
Subsection 32	Tests -1x decodes to the A Product network.
Subsection 33	Tests the -1x decodes to the A Product network and the upper bits of the Multiply Partial Summing network.
Subsection 34	Tests -0x decodes to the B Product network.
Subsection 35	Tests the -0x decodes to the B Product network and the upper bits of the Multiply Partial Summing network.
Subsection 36	Tests the -0x decodes to the A Product network.
Subsection 37	Tests the -0x decodes to the A Product network and the upper bits of the Multiply Partial Summing network.
Subsection 38	Tests C Register Sign control of complement decodes with decodes in C Register bits 67 through 73.
Subsection 39	Tests C Register Sign control of complement decodes with decodes in C Register bits 61 through 67.
Section 3	Checks Multiply Final Adder logic (ALN 2.5).
Subsection 0	Tests Multiply Final Adder for Enable detection in the bit 7 position.
Subsection 1	Tests Multiply Final Adder for Enable detection in the bit 6 position.

- Subsection 2 Tests Multiply Final Adder for Enable detection in the bits 5 through 0 positions.
- Subsection 3 Tests Multiply Final Adder Generate/Satisfy logic.
- Subsection 4 Tests Multiply Final Adder Generate/Enable/Satisfy logic.
- Subsection 5 Tests Multiply Final Adder Carry Interchange logic.
- Subsection 6 Tests Multiply Final Adder Logic for carry out of 12-bit iteration.
- Section 4 Checks B Register entry controls (ALN 2.4).
 - Subsection 0 Tests B Register 32-bit sign selection and extension.
 - Subsection 1 Tests B Register 48-bit entry, sign extended with bit 0 as sign.
 - Subsection 2 Tests Signed/Unsigned Multiply B Register Entry controls. The A and B Product networks for disable of B Register bit 0 fanout and disable of B and C Sign to the Product network recoders.
 - Subsection 3 Tests B Register entry of MSUM bits 8 through 71.
- Section 5 Checks C Register entry and 170 multiply controls (ALN 2.4).
 - Subsection 0 Tests C Register for copies of C Register bits from ADATC.
 - Subsection 1 Tests C Register entry of sign under 170 Mode Control.
 - Subsection 2 Tests B Register Sign Selection and Entry under 170 Mode Control.
 - Subsection 3 Tests Complement Correction signals for proper operation under 170 Mode Control.
- Section 6 Checks C Register entry, multiply/divide control and sign signals to the ALN general network and the Major Cycle Control Buffer (ALN 2.4).
 - Subsection 0 Tests the entry and shifting of MSUM bits 60 through 71 through the C Register.
 - Subsection 1 Tests Integer Multiply Overflow and the C Register and Multiply Final Adder zero checks.
 - Subsection 2 Tests 32-bit Integer Multiply Overflow detection.
 - Subsection 3 Tests multiply/divide unit for generation of Integer Multiply Divide Overflow and the ALN general network for encoding the overflow in the Normalize Encoder.
 - Subsection 4 Tests B and C Operand Sign Selection logic to form Multiply/Divide Sign and the enable of the Multiply/Divide Sign to the B and C Sign Fanouts that are sent to the ALN general network.

- Subsection 5 Tests sequencing of the Multiply/Divide Sign to the Internal Sign in the Micrand Register and the enable of the Internal Sign to the C Sign Fanouts.
- Subsection 6 Tests C Register Bit 7 XORed with Multiply/Divide Sign and extended through the ALN General Network Shifter.
- Subsection 7 Tests Major Cycle Control Buffer for holding of U4, U6 and U8.
- Subsection 8 Tests Major Cycle Control Buffer for holding of U1, U2 and U3.
- Section 7 Verifies operation of the Divide Quotient Register (ALN 2.6).
 - Subsection 0 Tests Divide Quotient Register for loading and its output through the C Register.
 - Subsection 1 Tests Divide Quotient Register for ones complement and a 1 place shift.
 - Subsection 2 Tests Divide Quotient Register for twos complement.
 - Subsection 3 Tests the Major Cycle Hold Register for Integer Divide Control, U7.
 - Subsection 4 Tests output of Divide Quotient Register for gating of Divide Fault and Divide Overflow.
 - Subsection 5 Tests Divide Overflow for select of right shift one in the ALN general network.
- Section 8 Checks Divisor and Remainder Register loading (ALN 2.6).
 - Subsection 0 Tests Divisor Register for 64-bit entry.
 - Subsection 1 Tests Divisor and Remainder Registers for 48-bit entry.
 - Subsection 2 Tests Divisor Register for 32-bit Integer entry.
 - Subsection 3 Tests Remainder Register load from the Quotient Register.
 - Subsection 4 Tests Divisor Register complement.
 - Subsection 5 Tests Remainder Register for entry of Remainder Output.
- Section 9 Checks Divide logic (ALN 2.6).
 - Subsection 0 Tests Divide logic and Carry Interchange.
 - Subsection 1 Tests Divide Carry Interchange logic.
 - Subsection 2 Tests Divide Round Control.

- Section 10** Checks Integer Divide operation and Pop Counter (ALN 2.5, 2.6).
- Subsection 0 Tests Integer entry to the Divide Remainder Register.
- Subsection 1 Tests upper Divide Arrays.
- Subsection 2 Tests Pop Counter.
- Section 11** Checks multiply/divide unit for error status reporting, parity checking and parity generation (ALN 2.4-2.6).
- Subsection 0 Tests C Register parity error detection and reporting.
- Subsection 1 Tests Parity toggle on C Register shift data entry.
- Subsection 2 Tests C Register parity generators and checkers.
- Subsection 3 Tests B Register parity error detection and reporting.
- Subsection 4 Tests B Register parity checkers and Multiply Final Adder parity generators.
- Subsection 5 Tests Multiply Carry error status reporting.

OIT3/P - Operand Issue (OPI) Test

- Section 0 Tests functional unit micrand immediate data (OPI 2.1).
 - Subsection 0 Tests literal register address R.F. write logic.
 - Subsection 1 Tests data path write width of 64 bits.
 - Subsection 2 Tests data path write width of 48 bits.
 - Subsection 3 Tests data path write width of 32 bits.
 - Subsection 4 Tests data path write width of 16 bits.
- Section 1 Tests register File read and Register File write (OPI 2.1).
 - Subsection 0 Tests RDSb Register File read address logic.
 - Subsection 1 Tests RDSb Data path to ALN.
 - Subsection 2 Tests RDSc Register File read address logic.
 - Subsection 3 Tests RDSc Data path to ALN.
- Section 2 Tests Operand Left Shift network (result to ALN) (OPI 2.3).
 - Subsection 0 Selects rightmost 32 Bits *2.
 - Subsection 1 Selects rightmost 32 Bits *8.
 - Subsection 2 Selects rightmost 18 Bits *8.
- Section 3 Tests 60-bit sign extension (OPI 2.3).
 - Subsection 0 Tests sign extension on B Operand (SEb Field).
 - Subsection 1 Tests sign extension on C Operand (SEc Field).
- Section 4 Tests Register File read of literal RDS data (OPI 2.1).
 - Subsection 0 Tests RDSb literal data path to ALN.
 - Subsection 1 Tests RDSc literal data path to ALN.
 - Subsection 2 Tests RDSa literal data path to Address Control.
- Section 5 Tests Live Register write/read (OPI 2.5).
 - Subsection 0 Tests write/read UCR.
 - Subsection 1 Tests write/read MCR.
- Section 6 Tests Live Register Write/Read (OPI 2.5).
 - Subsection 0 Tests Write/Read SIT.
 - Subsection 1 Tests Write/Read PIT.

- Section 7 Tests operand shift logic (result to Address Control) (OPI 2.3).
- Subsection 0 Select rightmost 18 bits *8; DS = 3.
- Section 8 Tests Largest Ring Check and Selection logic (OPI 2.3).
- Subsection 0 Tests data Mux to PVA Register (SM) Path through Largest Ring Select.
- Subsection 1 Tests DAI to Register File Path through Ring Select (WW = 1).
- Subsection 2 Tests DAI to Register File Path through Ring Select (WW = 3).
- Section 9 Tests Load Store Multiple Counters (OPI 2.4).
- Subsection 0 Tests N Counter.
- Subsection 1 Tests As Counter.
- Subsection 2 Tests Xs Counter.
- Subsection 3 Tests As/Xs parity logic.
- Section 10 Tests Load Store Multiple Counters (OPI 2.4).
- Subsection 0 Tests At using CC = 2 Load.
- Subsection 1 Tests Xt using CC = 2 Load.
- Subsection 2 Tests At using CC = 3 Load (also at < 2 Instruction Specification error).
- Subsection 3 Tests At using CC = 7 Load (also at < 2 Environment Specification error).
- Subsection 4 Tests At/Xt parity logic.
- Section 11 Tests Immediate Operand Mux 1 (OPI 2.1).
- Subsection 0 Tests Immediate Operand D input.
- Subsection 1 Tests Immediate Operand K input.
- Subsection 2 Tests Immediate Operand jk (C170) input.
- Subsection 3 Tests Immediate Operand jk (C180) input.
- Subsection 4 Tests Immediate Operand j (C180) input.
- Subsection 5 Tests Immediate Operand jkQ input.
- Subsection 6 Tests Immediate Operand Q input.
- Subsection 7 Tests C170 RAC Input.

Section 12 Tests address Control Immediate Data Mux (IDS Mux) (OPI 2.1).

Subsection 0 Tests Zero Data Constant generation.

Subsection 1 Tests constant = 8 hexadecimal generation.

Subsection 2 Tests D Zero Extended input.

Subsection 3 Tests Q Sign Extended input.

Subsection 4 Tests 8*D Zero Extended input.

Subsection 5 Tests 8*Q Sign Extended input.

Subsection 6 Tests 8*K Sign Extended input.

Subsection 7 Tests RDSB Save Register.

Section 13 Tests RAF write with RDS Fixed (RDSa) (OPI 2.3).

Subsection 0 Tests RAF = 0 (j).

Subsection 1 Tests RAF = 1 (k).

Subsection 2 Tests RAF = 2 (170i).

Subsection 3 Tests RAF = 4 (j+1).

Subsection 4 Tests RAF = 5 (k+1).

Subsection 5 Tests RAF = 6 (180i).

Section 14 Tests RAF read with RDS Fixed (RDSa) (OPI 2.3).

Subsection 0 Tests RAF = 0 (j).

Subsection 1 Tests RAF = 1 (k).

Subsection 2 Tests RAF = 2 (170i).

Subsection 3 Tests RAF = 4 (j+1).

Subsection 4 Tests RAF = 5 (k+1).

Subsection 5 Tests RAF = 6 (180i).

- Section 15 Tests RAF with RDS Varied (OPI 2.3).
- Subsection 0 Tests RAF during Register File Write using RDSd.
 - Subsection 1 Tests RAF during Register File Read using RDSa.
 - Subsection 2 Tests RAF during Register File Read using RDSb.
- Section 16 Tests RDS Bit 4 (OR bit) (OPI 2.3).
- Subsection 0 Tests OR Bit during Register File Write using RDSa.
 - Subsection 1 Tests OR Bit during Register File Write using RDSd.
 - Subsection 2 Tests OR Bit during Register File Read using RDSa.
 - Subsection 3 Tests OR Bit during Register File Read using RDSb.
 - Subsection 4 Tests OR Bit during Register File Read using RDSc.
- Section 17 Tests RDS BI Bits (bits 2 and 3) (OPI 2.3).
- Subsection 0 Tests BI Bits in RDS during write using RDSA.
 - Subsection 1 Tests BI Bits in RDS during write using RDSd.
 - Subsection 2 Tests BI Bits in RDS during read using RDSa.
 - Subsection 3 Tests BI Bits in RDS during read using RDSb.
 - Subsection 4 Tests BI Bits in RDS during read using RDSc.
- Section 18 Tests UZ check logic (no conflict) (OPI 2.3).
- Subsection 0 Tests UZ check logic using RDSc.
 - Subsection 1 Tests UZ check logic using RDSb.
 - Subsection 2 Tests UZ check logic using RDSa.
- Section 19 Tests sign extend local memory data (SEd) and Zero Fill RDSc logic (ZF) (OPI 2.3).
- Subsection 0 Tests logic controlled by SEd.
 - Subsection 1 Tests Zero Fill RDSc logic (ZF).
- Section 20 Tests parity logic; generators and associated checkers (OPI 2.0-2.5).
- Subsection 0 Tests parity network at Register File Address Minipipe.
 - Subsection 1 Tests parity network having generator at Literal Data input to Immediate Operand Mux 1.
 - Subsection 2 Tests parity network having generator at RDSw input to ICP.
 - Subsection 3 Tests parity network at Microsecond Counter.

- Section 21 Tests parity logic; detection and reporting of errors (OPI 2.0-2.5).
 - Subsection 0 Tests parity network at Register File Address Minipipe.
 - Subsection 1 Tests parity network having generator at Literal Data input to Immediate Operand Mux 1.
 - Subsection 2 Tests parity network having generator at RDSw input to ICP.
 - Subsection 3 Tests parity network at Microsecond Counter.
- Section 22 Tests parity networks having checkers in OPI; detection and reporting of errors (OPI 2.0-2.5).
 - Subsection 0 Tests RDSw parity logic.
 - Subsection 1 Tests Virtual Instruction data parity logic.
- Section 23 Tests block Register File write (OPI 2.1).
 - Subsection 0 Tests block Register File write on DAI parity error.
- Section 24 Tests Minipipe comparators (no compare) (OPI 2.0).
 - Subsection 0 Tests Rank 40 and Rank 50 comparators.

PDT3/P - Processor Detected Malfunction and Associated Logic Test (ICC 2.0)

Section 0	Tests MCR and UCR.
	Subsection 0 Tests the MCR and UCR with live register writes.
Section 1	Tests MCR.
	Subsection 0 Tests Outward Call/Inward Return.
	Subsection 1 Tests Invalid Segment/Ring 0.
	Subsection 2 Tests SIT.
	Subsection 3 Tests Page Table Search without Find.
	Subsection 4 Tests access violation.
	Subsection 5 Tests address specification error.
	Subsection 6 Tests instruction specification error.
	Subsection 7 Tests environment specification error.
Section 2	Tests detected uncorrectable error.
	Subsection 0 Tests Address Control before PONR PDM.
	Subsection 1 Tests general micrand parity fault.
	Subsection 2 Tests Load Register parity fault.
	Subsection 3 Tests IF PDM.
	Subsection 4 Tests BDP Convert Error to MCR(0).
	Subsection 5 Tests BDP Input PE to MCR(0).
Section 3	Tests UCR.
	Subsection 0 Tests Invalid BDP data.
	Subsection 1 Tests Arithmetic Loss of Significance.
	Subsection 2 Tests FP Indefinite.
	Subsection 3 Tests FP Loss of Significance.
	Subsection 4 Tests Exponent Underflow.
	Subsection 5 Tests Exponent Overflow.
	Subsection 6 Tests Arithmetic Overflow.
	Subsection 7 Tests Divide Fault.
	Subsection 8 Tests Inter-ring Pop.
	Subsection 9 Tests PIT.

Section 4 Tests C170 Exit Mode Register.

Subsection 0 Tests C170 Indefinite Operand.

Subsection 1 Tests C170 Infinite Operand.

Subsection 2 Tests C170 Operand AOR.

Subsection 3 Tests C170 RNI AOR.

Subsection 4 Tests C170 Illegal Instruction.

Subsection 5 Tests C170 address correct if held up.

Section 5 Tests parity detection logic.

Subsection 0 Tests P Register parity detection in ICP.

Subsection 1 Tests UTP parity detection in ICP.

Subsection 2 Tests PDM on Page Table errors.

SMT3/P - Segment Map (SM) Test (SM 2.0)

- Section 0 Tests basic paths.
 - Subsection 0 Tests the PVA input via parity status.
 - Subsection 1 Tests setting of the UVMID flag.
 - Subsection 2 Tests the Segment Descriptor Mux, Gate 3.
 - Subsection 3 Tests the PVA register, New P Register and Old P Register.
 - Subsection 4 Tests the Old P Register input to the Global Key Input Mux.
- Section 1 Tests the ring compare logic.
 - Subsection 0 Tests the R2 ring compare logic.
 - Subsection 1 Tests the largest ring compare logic.
 - Subsection 2 Tests the Old P RN input to the R1/PVA RN Mux and the PVA RN input to the PVA/OLD P RN Mux.
 - Subsection 3 Tests the Ring Hold Register and the ring hold compare logic.
 - Subsection 4 Tests the inter-ring compare logic.
- Section 2 Tests segment validity logic.
 - Subsection 0 Tests segment validity logic via a CALL1 microfunction.
 - Subsection 1 Tests segment validity.
 - Subsection 2 Tests global key/lock test logic.
 - Subsection 3 Tests the local key/lock test logic.
- Section 3 Tests map read/write support logic.
 - Subsection 0 Tests the monitor/job status RAMs.
 - Subsection 1 Tests the segment map set 0,1 hit compare logic.
 - Subsection 2 Tests the set 0,1 write select translator logic.
 - Subsection 3 Tests the status RAM update control logic.
 - Subsection 4 Tests the status RAMs for address uniqueness.
- Section 4 Tests the Map sets.
 - Subsection 0 Tests the segment number portion of Map set 0 and 1.
 - Subsection 1 Tests the Map set 0,1 RAM bits 0 through 47 and parity.

Section 5 Tests segment table address.

- Subsection 0 Tests the segment table address register.
- Subsection 1 Tests the segment table address save register.
- Subsection 2 Tests the status RAM purge control logic.
- Subsection 3 Tests the segment table length test logic.

Section 6 Tests PDMs generated by segment Map.

- Subsection 0 Tests the SMPDM with NEW P, VMID and CBP R3 parity errors.
- Subsection 1 Tests the SMPDM by forcing STL parity errors.
- Subsection 2 Tests the SMPDM by forcing micrand parity errors.
- Subsection 3 Tests the SPDMBP by forcing Segment Descriptor Mux parity errors.
- Subsection 4 Tests the SPDMBP by forcing PVA parity errors.
- Subsection 5 Tests the SPDMBP by forcing Status RAM errors.
- Subsection 6 Tests the Disable PDM's control in Segment Map.

Section 7 Tests miscellaneous logic.

- Subsection 0 Tests SM control of LM purges.

Maintenance Register Codes

B

Maintenance Register Bit Descriptions	B-2
SS Register (00)	B-2
EID Register (10)	B-3
CPU OI Register (12)	B-3
CPU DEC Register (30)	B-4
CPU CSA Register (31)	B-5
CPU PFS0 Register (80)	B-6
CPU PFS1 Register (81)	B-7
CPU PFS2 Register (82)	B-8
CPU PFS3 Register (83)	B-9
CPU PFS4 Register (84)	B-10
CPU PFS5 Register (85)	B-11
CPU PFS6 Register (86)	B-12
CPU PFS7 Register (87)	B-13
CPU PFS8 Register (88)	B-14
CPU PFS9 Register (89)	B-14
CPU PTM Register (A0)	B-15
CMC OI Register (12)	B-16
CMC EC Register (20)	B-17
CMC BC Register (21)	B-18
CMC CEL Register (A0)	B-18
CMC UEL1 Register (A4)	B-19
CMC UEL2 Register (A8)	B-20
CMC FRC Register (B0)	B-20
IOU 960 (NIO), 962 (CIO) OI Register (12)	B-21
IOU 960 (NIO), 962 (CIO) FSM Register (18)	B-22
IOU 960 (NIO), 962 (CIO) OSB Register (21)	B-22
IOU 960 (NIO), 962 (CIO) EC Register (30)	B-23
IOU 960 (NIO), 962 (CIO) S Register (40)	B-24
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Maintenance Register Codes

B

This appendix provides bit descriptions for all central processing unit (CPU), central memory control (CMC), and input/output unit (IOU) maintenance registers. This appendix also includes IOU error isolation procedures related to maintenance registers 80, 81, 84, and 85. Detailed bit definitions are provided for the following IOU and CMC maintenance registers.

Register	Description
80	IOU Fault Status Register 1 for 960 NIO and 962
81	IOU Fault Status Register 2 for 960 NIO and 962
84	IOU Fault Status Register 1 for 960 CIO
85	IOU Fault Status Register 2 for 960 CIO
A0	CMC Corrected Error Log
A4	CMC Uncorrectable Error Log 1
A8	CMC Uncorrectable Error Log 2

Maintenance Register Bit Descriptions

SS Register (00)

Byte	Bit(s)	IOU	CMC	CPU
0	00-07	(Not used)	(Not used)	(Not used)
1	08-15	(Not used)	(Not used)	(Not used)
2	16-23	(Not used)	(Not used)	(Not used)
3	24-31	(Not used)	(Not used)	(Not used)
4	32-39	(Not used)	(Not used)	(Not used)
5	40-47	(Not used)	(Not used)	(Not used)
6	48-55	(Not used)	(Not used)	(Not used)
7	56	(Not used)	Osc selected ²	(Not used)
	57	CMI dsbl status ¹	Osc selected ²	(Not used)
	58	Short warning ¹	(Not used)	C180 monitor mode
	59	Summary status	(Not used)	Short warning
	60	Processor halt	Early warning	Processor halt
	61	Uncor error	Uncor error	Uncor error
	62	Cor error	Cor error	Cor error
	63	Long warning	Long warning	Long warning

Notes:

1. 962 only.

2. Bits 56 and 57 are decoded as follows.

56	57	Percent
0	0	Normal
1	0	+2
0	1	-2

EID Register (10)

Element	Element No. (Bits 32-39)	Model No. (Bits 40-47)
Central Processor	00	3A
Central Memory	01	34
Input/Output Unit	02	40 (960), 44 (962)

NOTE

Bits 48-63 contain the element serial number.

CPU OI Register (12)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-47	(Not used)
6	48-55	(Not used)
7	56-61	(Not used)
	62	32K-byte cache installed (constant logic 1)
	63	(Not used)

CPU DEC Register (30)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32	Enbl shadow memory
	33	Test mode enbld
	34	Enbl first failure capture
	35	Disbl cor error
	36-39	Page map configuration, enbl set 0-3
5	40,41	Seg map configuration, enbl set 0,1
	42	CST RAM sweep enbl
	43	Enbl PDM halt
	44	CST bkpt enbl
	45	Instr step enbl
	46	Enbl expanded CST
	47	Dsbl PDMs
6	48	CST expansion (future use)
	49	(Not used)
	50	Enbl cache lookahead (dsbld)
	51	Enbl block request
	52-55	Error retry limit
7	56	Error retry limit parity
	57-60	Cache configuration, enbl set 0-3
	61	Cache fake central mem
	62	Force real mem adrs
	63	(Not used)

CPU CSA Register (31)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-47	(Not used)
6	48-52	(Not used)
6,7	53-63	CSA

CPU PFS0 Register (80)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Module	Diagram	Description
0	00	IFIC	ICC 2.0	R60 after PONR MCR bit 0: uncor PE
	01	IFIC	ICC 2.0	Cor/soft/bypass error, MAC opn PDM
	02,03	OPSM	OPI 2.5	AC adrs mux to LM PE, byte 2,3
	04-07	AC	AC 2.3	AC adrs mux to LM PE, byte 4-7
1	08-15	AC	AC 2.0	A/C stream data assy rgtr PE, byte 0-7
2	16-23	AC	AC 2.0	A/C stream data bfr rgtr PE, byte 0-7
3	24-31	AC	AC 2.1	B stream data bfr rgtr PE, byte 0-7
4	32,33	OPSM	OPI 2.5	A/C stream ASID rgtr PE, byte 0,1
	34,35	OPSM	OPI 2.5	B stream ASID rgtr PE, byte 0,1
	36,37	AC	AC 2.2	Address offset sel mux PE, byte 2,3
	38,39	AC	AC 2.1	AC micr PE, byte 0,1
5	40-43	AC	AC 2.3	Recovery adrs rgtr PE, byte 0-3
	44	ALN	ALN 2.6	ALN soft cont data-out rgtr PE
	45,46	AC	AC 2.1	AC soft cont 2,1 data-out rgtr PE
	47	AC	AC 2.2	ALN shift count rgtr PE
6	48	AC	AC 2.1	A/C stream length cntr PE
	49	AC	AC 2.1	B stream length cntr PE
	50	AC	AC 2.0	A stream data byte to BDP PE
	51	AC	AC 2.1	B stream data byte to BDP PE
	52	AC	AC 2.0	Store bit/all other opn sel mux PE
	53	ALN	ALN 2.0	Conv-to-binary data byte from BDP PE
	54,55	BDP	BDP 2.3	B,A stream stage 1 data rgtr PE
7	56,57	BDP	BDP 2.3	Rgtr file A,B adrs cntr PE
	58,59	BDP	BDP 2.3	Rgtr file A,B data PE
	60	BDP	BDP 2.3	Dec adder bits 10-17, conv-to-dec PE
	61	BDP	BDP 2.3	Table load limit rgtr stage 3 PE
	62	BDP	BDP 2.3	Common stage 7 rgtr PE
	63	CSMC	MAC 2.0	PFS board O int PE

CPU PFS1 Register (81)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Module	Diagram	Description
0	00	BDP	BDP 2.3	Buffer RAM adrs cntr PE
	01	BDP	BDP 2.3	C stream stage 2 data rgtr PE
	02	BDP	BDP 2.3	Spec error RAM, x256 RAM adrs PE
	03	BDP	BDP 2.3	Spec error RAM, x256 RAM out data PE
	04	BDP	BDP 2.3	A stream stage 2 data rgtr PE
	05	BDP	BDP 2.3	B stream stage 2 data rgtr PE
	06	BDP	BDP 2.3	Aj descr PE
	07	BDP	BDP 2.3	Ak descr PE
1	08	BDP	BDP 2.3	Translate RAM adrs PE
	09	BDP	BDP 2.3	Translate RAM output data PE
	10	BDP	BDP 2.3	Conv-to-binary/dec RAM adrs PE
	11	BDP	BDP 2.3	Conv-to-binary/dec RAM output data PE
	12	BDP	BDP 2.3	BDP micr byte 0 or 1 PE
	13	BDP	BDP 2.3	BDP micr byte 2 or 3 PE
	14	BDP	BDP 2.3	BDP micr byte 4 or 5 PE
	15	BDP	BDP 2.3	BDP micr byte 6 or 7 PE
2	16	AC	CLK 2.0	AC clk array PE
	17	CMCB	CLK 2.0	CMCB clk array PE
	18	1	CLK 2.0	CSU clk array PE
	19-23			(Not used)
3	24-31			(Not used)
4	32-39			(Not used)
5	40-47			(Not used)
6	48-55			(Not used)
7	56-63			(Not used)

Note:

1. CM Interface Module.

CPU PFS2 Register (82)

Byte	Bit(s)	Module	Diagram	Description
0	00	BDP	BDP 2.3	Immed data byte in scale cntr PE
	01	BDP	BDP 2.3	Edit mask byte rgtr PE
	02-07	LMA	LM 2.0	Cache adrs rgtr PE, byte 0-5
1	08-15	LMA	LM 2.0	Cache write-data PE, byte 0-7
2	16	LMA	LM 2.0	Multiple cache hit
	17	LMA	LM 2.0	Multiple cache allocate error
	18	LMB	LM 2.1	Cache tag file PE
	19	LMB	LM 2.1	Cache tag file adrs PE
	20	OPSM	SM 2.0	DAI PE: LM read data mux, direct CMC data 3
	21	OPSM	SM 2.0	DAI PE: LM read data mux, cache read data 2
	22	OPSM	SM 2.0	DAI PE: LM read data mux, real memory adrs 1
	23	OPSM	SM 2.0	DAI PE: LM read data mux, bfr CMC data 0
3	24	LMA	LM 2.0	Cache write data from CPU PE
	25	LMA	LM 2.0	Cache block fill data from CM port PE
	26	LMA	LM 2.0	Cache adrs rgtr PE 4: cache associative tag
	27	LMA	LM 2.0	Cache mark data PE
	28	LMA	LM 2.0	Cache adrs rgtr PE: adrs mux 0: invalidate
	29	LMA	LM 2.0	Cache adrs rgtr PE: adrs mux 1: AC adrs
	30	LMA	LM 2.0	Cache adrs rgtr PE: adrs mux 2: IF adrs
	31	LMA	LM 2.0	Cache adrs rgtr PE: adrs mux 3: interrupt
4	32	LMA	LM 2.0	Modified purge code (from SM) PE
	33	LMA	LM 2.0	LM micr PE, byte 0
	34	LMA	LM 2.0	LM micr PE, byte 1
	35			(Not used)
	36-39	LMA	LM 2.0	Page map status PE, set 0-3
5	40-43	LMA	LM 2.0	Page map PE, set 0-3
	44	LMA	LM 2.0	Page frame adrs PE
	45-47			(Not used)
6	48	LMA	LM 2.0	Page table length rgtr PE
	49	LMA	LM 2.0	Page table adrs rgtr PE
	50	LMA	LM 2.0	Page offset rgtr PE
	51	LMA	LM 2.0	Page size mask PE
	52	LMA	LM 2.0	Stream mode exchange word tag PE
	53-55			(Not used)

Byte	Bit(s)	Module	Diagram	Description
7	56	LMA	LM 2.0	CMC response 2: cor error write
	57	LMA	LM 2.0	CMC response 6: cor error read
	58	LMA	LM 2.0	CMC response 1: uncor error write
	59	LMA	LM 2.0	CMC response 5: uncor error read
	60	LMA	LM 2.0	CMC response 7: reject
	61	LMA	LM 2.0	CMC response code: PE
	62	LMB	LM 2.1	CMC tag rgtr PE
	63	CSMC	MAC 2.0	PFS board 1 int PE

CPU PFS3 Register (83)

Byte	Bit(s)	Module	Diagram	Description
0	00-03	LMA	LM 2.0	Cache adrs PE, set 0-3
	04-07	LMA	LM 2.0	Cache tag RAM PE, set 0-3
1	08-11	OPSM	SM 2.0	DAI PE, cache data, set 0-3
	12	OPSM	SM 2.0	DAI PE: DAI mux, local mem read data 3
	13	OPSM	SM 2.0	DAI PE: DAI mux, byte load data 2
	14	OPSM	SM 2.0	DAI PE: DAI mux, ALN result data 1
	15	OPSM	SM 2.0	DAI PE: DAI mux, functional unit micr 0
2	16	LMA	CLK 2.0	LMA clk array PE
	17	LMB	CLK 2.0	LMB clk array PE
	18	CMCA	CLK 2.0	CMCA clk array PE
	19-23			(Not used)
3	24-31			(Not used)
4	32-39			(Not used)
5	40-47			(Not used)
6	48-55			(Not used)
7	56-63			(Not used)

CPU PFS4 Register (84)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Module	Diagram	Description
0	00,01	OPSM	SM 2.0	Seg descr mux-out PE, set 0,1
	02-07	OPSM	SM 2.0	Seg descr mux PE, byte 0-5
1	08,09	OPSM	SM 2.0	Seg table length PE, byte 0,1
	10	OPSM	SM 2.0	Seg table adrs rgtr PE, bytes 0 and 3
	11	OPSM	SM 2.0	Seg table adrs rgtr PE, bytes 1 and 2
	12-15	OPSM	SM 2.0	New P rgtr PE, byte 0-3
2	16	OPSM	SM 2.0	PVA rgtr bits 4-7 (CBP VMID) PE
	17	OPSM	SM 2.0	PVA rgtr bits 12-15 (CBP R3) PE
	18,19	OPSM	SM 2.0	PVA rgtr PE, byte 2,3
	20	OPSM	SM 2.0	Seg descr mux-out PE: neither set sel
	21	OPSM	SM 2.0	Valid status RAM error: PE or double hit
	22,23	OPSM	SM 2.0	SM micr PE, byte 0,1
3	24	OPSM	SM 2.0	Purge code PE
	25	IFIC	ICP 2.0	Rank 32 BDP descr data type rgtr PE
	26	IFIC	ICP 2.0	Rank 32 j,k rgtr PE
	27-31	IFIC	ICP 2.0	Rank 50 UTP rgtr PE, byte 2-7
4	32,33	IFIC	ICP 2.0	Live rgtr write-data PE, byte 0,1
	34	IFIC	ICP 2.0	Rank 41 general micr PE 2, byte 3
	35	IFIC	ICP 2.0	Rank 41 general micr PE 1, byte 2
	36-39	IFIC	ICP 2.0	Rank 50 P rgtr PE, byte 4-7
5	40	IFIC	ICP 2.0	Rank 41 general micr PE 3 (byte 4)
	41	IFIC	ICC 2.0	Successful retry
	42	IFIC	ICP 2.0	Deadman time-out
	43	IFIC	ICP 2.0	Debug mask PE
	44	IFIC	ICC 2.0	MAC opn PDM
	45	IFIC	ICP 2.0	Retry cntr rgtr PE
	46	IFIC	ICC 2.0	PDM during exchange (exchange mode set)
	47	IFIC	ICP 2.0	Rank 50 before PONR PDM
6	48-55	OPIA	OPI 2.3	DAI PE 1-8: rgtr file write data PE, byte 0-7
7	56	OPIA	OPI 2.0	Minipipe rank 50 rgtr file write adrs PE
	57	OPIB	OPI 2.1	Rgtr file read data rgtr PE, bytes 0-3
	58	OPIB	OPI 2.1	Rgtr file read data rgtr PE, bytes 4-7
	59	OPSM	OPI 2.5	CMC tag (from LM) PE
	60-62			(Not used)
	63	CSMC	MAC 2.0	PFS board 2 int PE

CPU PFS5 Register (85)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Module	Diagram	Description
0	00-03	OPSM	OPI 2.5	Rank 22 P rgtr PE, byte 4-7
	04	OPSM	OPI 2.5	R22 BDP descr data type field PE
	05	OPSM	OPI 2.5	Rank 22 j,k field PE
	06,07	OPSM	OPI 2.5	Rank 22 immed operand PE, byte 0,1
1	08,09	OPSM	OPI 2.5	Functional unit micr PE, byte 6,7
	10,11	OPSM	OPI 2.5	Rgtr data sel write field PE, byte 0,1
	12	OPSM	OPI 2.5	Increment j,k field PE
	13-15			(Not used)
2	16	OPSM	CLK 2.0	OPSM clk array PE
	17	OPIB	CLK 2.0	OPIB clk array PE
	18	OPIA	CLK 2.0	OPIA clk array PE
	19-23			(Not used)
3	24-31			(Not used)
4	32-39			(Not used)
5	40-47			(Not used)
6	48-55			(Not used)
7	56-63			(Not used)

CPU PFS6 Register (86)

Byte	Bit(s)	Module	Diagram	Description
0	00-02			(Not used)
	03	CSMC	CST 2.0	Micrand adrs rgtr PE
	04,05	CSMC	MAC 2.0	CST write data (from MAC) PE, byte 0,1
	06,07	CSMC	CST 2.0	MSC field rgtr PE, byte 0,1
1	08-15	CSMC	CST 2.0	FU micr bfr rgtr (t23) PE, byte 0-7
2	16-23	CSMC	CST 2.0	FU micr rgtr (t31) PE, byte 0-7
3	24-29	CSMC	CST 2.0	General micr rgtr (t22) PE, byte 2-7
	30	OPSM	OPI 2.4	A-start, X-start cntr rgtr PE
	31	OPSM	OPI 2.4	A-terminate, X-terminate cntr rgtr PE
4	32	CSMC	MAC 2.0	Maint chan out rgtr (to IOU) PE
	33	CSMC	MAC 2.0	Maint chan input: write data or fcfn word PE
	34	CSMC	MAC 2.0	Maint chan input: data fanout PE
	35	CSMC	MAC 2.0	Read data (to maint chan out rgtr) mux PE
	36	CSMC	MAC 2.0	Reference ROM adrs PE
	37	CSMC	MAC 2.0	Address translation mux PE
	38	CSMC	MAC 2.0	Reference ROM data PE
	39	OPSM	OPI 2.4	N cntr rgtr PE
5	40	IFIC	IF 2.1	First level instr C170 odd RAM A PE
	41	IFIC	IF 2.1	First level instr C170 even RAM A PE
	42	IFIC	IF 2.1	First level instr C180 RAM A PE
	43	IFIC	IF 2.1	IB12 P rgtr, byte 4
	44	IFIC	IF 2.1	IB12 P rgtr, byte 5
	45	IFIC	IF 2.1	Rank 12 instr bfr opcode
	46	IFIC	IF 2.1	IB12 instr mux bits 3, 12-15, 24
	47	IFIC	IF 2.1	IB12 instr mux bits 16-23
6	48	IFIC	IF 2.1	First level instr C170 odd RAM B PE
	49	IFIC	IF 2.1	First level instr C170 even RAM B PE
	50	IFIC	IF 2.1	First level instr C180 RAM B PE
	51	IFIC	IF 2.1	IB12 P rgtr, byte 6
	52	IFIC	IF 2.1	IB12 P rgtr, byte 7
	53	IFIC	IF 2.1	IB12 P instr mux bits 33-40
	54	IFIC	IF 2.1	IB12 P instr mux bits 25-32
	55			(Not used)
7	56-59	IFIC	IF 2.0	Branch adrs A rgtr PE, byte 0-3
	60-62	IFIC	IF 2.0	Branch adrs B rgtr PE, byte 1-3
	63	CSMC	MAC 2.0	PFS board 3 int PE

CPU PFS7 Register (87)

Byte	Bit(s)	Module	Diagram	Description
0	00-03	IFIC	IF 2.1	Branch adrs adder input PE, byte 0-3
	04-07	IFIC	IF 2.0	Branch adrs rgtr PE, byte 4-7
1	08	IFIC	IF 2.1	IB02 PE, byte 0; Instr mux bits 3, 12-15, 24
	09	IFIC	IF 2.1	IB02 PE, byte 1; Instr mux bits 16-23
	10	IFIC	IF 2.1	IB02 PE, byte 2; Instr mux bits 25-32
	11	IFIC	IF 2.1	IB02 PE, byte 3; Instr mux bits 33-40
	12	IFIC	IF 2.1	IB11 PE, byte 0; Instr mux bits 3, 12-15, 24
	13	IFIC	IF 2.1	IB11 PE, byte 1; Instr mux bits 16-23
	14	IFIC	IF 2.1	IB11 PE, byte 2; Instr mux bits 25-32
	15	IFIC	IF 2.1	IB11 PE, byte 3; Instr mux bits 33-40
2	16	IFIC	CLK 2.0	IFIC clk array PE
	17	CSMC	CLK 2.0	CSMC clk array PE
	18	BDP	CLK 2.0	BDP clk array PE
	19	AC	MAC 2.0	First failure detected in rgtr 80/81
	20	LMA	MAC 2.0	First failure detected in rgtr 82/83
	21	OPSM	MAC 2.0	First failure detected in rgtr 84/85
	22	IFIC	MAC 2.0	First failure detected in rgtr 86/87
	23	ALN	MAC 2.0	First failure detected in rgtr 88/89
3	24-31			(Not used)
4	32-39			(Not used)
5	40-47			(Not used)
6	48-55			(Not used)
7	56-63			(Not used)

CPU PFS8 Register (88)

Byte	Bit(s)	Module	Diagram	Description
0	00-07	IFIC	IF 2.1	Instr assy rgtr PE, byte 0-7
1	08,09	IFIC	IF 2.1	Parcel 3 save rgtr PE, byte 0,1
	10-13	IFIC	IF 2.1	P mux PE, byte 0-3
	14,15	ALN	ALN 2.0	Mult/div minor cycle cont rgtr PE, byte 0,1
2	16-23	ALN	ALN 2.4	C rgtr data PE, byte 0-7
3	24-31	ALN	ALN 2.0	B rgtr data PE, byte 0-7
4	32-39	ALN	ALN 2.3	Large adder input PE, byte 0-7
5	40-43	ALN	ALN 2.3	Large adder input PE, byte 8-11
	44-47	ALN	ALN 2.3	Large adder byte 0-3 carry error
6	48-55	ALN	ALN 2.3	Large adder byte 4-11 carry error
7	56,57			(Not used)
	58,59	ALN	ALN 2.0	Shift count (from AC) PE, byte 0,1
	60,61	ALN	ALN 2.0	Multiply final adder carry error, byte 0,1
	62			(Not used)
	63	CSMC	MAC 2.0	PFS board 4 int PE

CPU PFS9 Register (89)

Byte	Bit(s)	Module	Diagram	Description
0	00-06	ALN	ALN 2.0	Multiply final adder carry error, byte 2-8
	07			(Not used)
1	08-15	ALN	ALN 2.0	ALN micr PE, byte 0-7
2	16	ALN	CLK 2.0	ALN clk array PE
	17	MD	CLK 2.0	MD clk array PE
	18	MD	CLK 2.0	MD clk array PE
	19-23			(Not used)
3	24-31			(Not used)
4	32-39			(Not used)
5	40-47			(Not used)
6	48-55			(Not used)
7	56-63			(Not used)

CPU PTM Register (A0)

Byte	Bit(s)	Description
0	00	Address cont, data to length cntr
	01	Address cont, 8-bit adder
	02	Address cont, ALN shift count
	03	BDP, AJ port formatting
	04	BDP, AK port formatting
	05	BDP, scan rgtr file adrs
	06	BDP, spec error ROM adrs
	07	BDP, encode
1	08	Test retry hardware
	09	Address cont, mark lines
	10	Local mem, page offset
	11	Local mem, seg/page identifier
	12	Operand issue, write adrs pipeline input
	13	Operand issue, data subfctn sel
	14	Operand issue, literal data
	15	Instr fetch, instr decode muxes
2	16	ALN, force C rgtr PE
	17	ALN, force shift fault
	18	MAC, data output force 0 parity
	19	CMC partial parity dsbl
	20	CSU partial parity dsbl
	21	(Not used)
	22	LM, purge adrs cntr parity invert
	23	LM, page map status parity invert, set 0
3	24-26	LM, page map status parity invert, set 1-3
	27	LM, tag file parity invert
	28	LM, LM tag to CMC parity invert
	29	CMC response code parity invert
	30,31	LM, RMA parity invert bytes 0, 1
4	32,33	LM, RMA parity invert bytes 2, 3
	34	LM fctn code CMC parity invert
	35	Operand issue, data subfctn sel (companion with bit 13)
	36	Operand issue, force PE on RDSW to instr cntr
	37	Operand issue, force PE on microsecond cntr
	38	(Not used)
	39	Force cache set 1 allocate
5	40-42	Set tag file 0-2 full
	43	Force LRU parity=0 on cache tag
	44	Force LM tag error
	45-47	(Not used)
6	48-55	(Always zero)
7	56-63	(Always zero)

CMC OI Register (12)

Byte	Bit(s)	Description
0	00	Memory size = 2GB
	01	Memory size = 1GB
	02	Memory size = 512MB
	03	Memory size = 256MB
	04	Memory size = 128MB
	05	Memory size = 64MB
	06	Memory size = 32MB
	07	Memory size = 16MB
1	08	Memory size = 8MB
	09	Memory size = 4MB
	10	Memory size = 2MB
	11	Memory size = 1MB
	12	Enbl relocate RMA area 0000 of CM
	13-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-47	(Not used)
6	48-55	(Not used)
7	56-63	(Not used)

CMC EC Register (20)

Byte	Bit(s)	Description
0	00	Dsbl parity checking
	01	Dsbl SECEDED
	02	00 Normal (Check byte/syndrome control)
	03	01 Write byte 0
		10 Read byte 0
		11 Read syndrome
	04	Timing margins
	05	00 Normal
		01 Narrow
		10 Wide
		11 Wide
	06	Fast clock margins
	07	Slow clock margins
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32	Port dsbl on CP-0
	33	Port dsbl on IOU-0
	34	Port dsbl on CP-1
	35	Port dsbl on IOU-1
	36	Sel lower (set) or upper (clear) address bounds limit
	37	Enbl refresh
	38	Dsbl cor error reporting to ports
	39	Dsbl single bit errors
5	40-47	(Not used)
6	48-55	(Not used)
7	56-63	(Not used)

CMC BC Register (21)

Byte	Bit(s)	Description
0	00	Bounds enable CP-0
	01	Bounds enable IOU-0
	02	Bounds enable CP-1
	03	Bounds enable IOU-1
	04-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-44	(Not used)
	45-47	Bounds address bits 1-3
6	48-55	Bounds address bits 4-11
7	56-63	Bounds address bits 12-19)

CMC CEL Register (A0)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Description
0	00	Valid bit
	01	Unlogged corrected error
	02-07	(Not used)
1	08	(Not used)
	09-11	Port code bits 0-2 (0=CP-0, 1=IOU-0, 2=CP-1, 3=IOU-1)
	12-15	CM address bits 1-4
2	16-23	CM address bits 5-12
3	24-31	CM address bits 13-20
4	32-39	CM address bits 21-28
5	40-43	CM address parity bits 0-3
	44-47	(Not used)
6	48-55	Syndrome code bits 0-7
7	56-63	(Not used)

CMC UEL1 Register (A4)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Description
0	00	Valid bit
	01	Unlogged uncor error
	02	Multiple-bit error
	03-06	Function code bits 0-3
	07	Function code parity bit
1	08	Mark parity bit
	09-11	Port code bits 0-2 (0=CP-0, 1=IOU-0, 2=CP-1, 3=IOU-1)
	12-15	CM address bits 1-4
2	16-23	CM address bits 5-12
3	24-31	CM address bits 13-20
4	32-39	CM address parity bits 21-28
5	40-43	CM address parity bits 0-3
	44-47	Parity error code bits 0-3 ¹
6	48-55	Write parity error bytes 0-7
7	56-63	Mark bits 0-7

Note:

1. Bits 44 through 47 are decoded as follows.

Bits	Description
1111	CM address byte 3 parity error II
1110	CM address byte 2 parity error II
1101	CM address byte 1 parity error II
1100	CM address byte 0 parity error II
1011	CM address byte 3 parity error I
1010	CM address byte 2 parity error I
1001	CM address byte 1 parity error I
1000	CM address byte 0 parity error I
0111	CM address byte 3 parity error
0110	CM address byte 2 parity error
0101	CM address byte 1 parity error
0100	CM address byte 0 parity error
0011	Tag parity error
0010	Mark parity error
0001	Function code parity error
0000	No error

CMC UEL2 Register (A8)

(Refer to detailed bit definitions later in this appendix.)

Byte	Bit(s)	Description
0	00	Valid bit
	01	Unlogged uncorrectable error
	02	Illegal function
	03	Bounds fault
	04	Write data byte 7 parity error
	05-07	(Not used)
1	08	(Not used)
	09-11	Port code bits 0-2 (0=CP-0, 1=IOU-0, 2=CP-1, 3=IOU-1)
	12-15	CM address bits 1-4
2	16-23	CM address bits 5-12
3	24-31	CM address bits 13-20
4	32-39	CM address bits 21-28
5	40-43	CM address parity bits 0-3
	44-47	(Not used)
6	48-55	Read data parity error bytes 0-7
7	56-63	Partial write data parity error bytes 0-7

CMC FRC Register (B0)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2-7	16-63	48-bit counter (Increments once each microsecond.)

IOU 960 (NIO), 962 (CIO) OI Register (12)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-19	(Not used)
	20	Barrel 3, PP25-31
	21	Barrel 2, PP20-24
	22	Barrel 1, PP5-11
	23	Barrel 0, PP0-4
3	24-31	Channels 7-0
4	32	Channel 17
	33	(Not used)
	34	Channel 15
	35	(Not used)
	36-39	Channels 13-10
5	40-47	Channels 27-20
6	48-51	Channel code bits 0-3
	52-55	Channels 33-30
7	56	CIO (not used on 962)
	57-60	(Not used)
	61	Radial interface 1,2,3
	62	Two-port mux
	63	(Not used)

IOU 960 (NIO), 962 (CIO) FSM Register (18)

Byte	Bit(s)	Description
0	00-02	(Not used)
	03-07	Mask vector, barrel 0 PP4-0
1	08-10	(Not used)
	11-15	Mask vector, barrel 1 PP4-0
2	16-18	(Not used)
	19-23	Mask vector, barrel 2 PP4-0
3	24-26	(Not used)
	27-31	Mask vector, barrel 3 PP4-0
4	32-39	Mask vector, channel 7-0
5	40	Mask vector, channel 17
	41	(Not used)
5	42	Mask vector, channel 15
	43	(Not used)
	44-47	Mask vector, channel 13-10
6	48-55	Mask vector, channel 27-20
7	56	MAC mask vector
	57,58	(Not used)
	59	Mask vector, radial interface 1/2/3
	60-63	Mask vector, channel 33-30

IOU 960 (NIO), 962 (CIO) OSB Register (21)

Byte	Bit(s)	Description
0	00-02	(Not used)
	03-07	Bit vector, barrel 0 PP4-0
1	08-10	(Not used)
	11-15	Bit vector, barrel 1 PP4-0
2	16-18	(Not used)
	19-23	Bit vector, barrel 2 PP4-0
3	24-26	(Not used)
	27-31	Bit vector, barrel 3 PP4-0
4	32-39	(Not used)
5	40-45	(Not used)
	46,47	OS boundary adrs bits 36,37
6	48-55	OS boundary adrs bits 38-45
7	56-63	OS boundary adrs bits 46-53

IOU 960 (NIO), 962 (CIO) EC Register (30)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32	8K PP memory
	33	System initialized
	34	(Not used)
	35-39	PP number
5	40-42	(Not used)
	43-47	Chan number
6	48-50	(Not used)
	51	Load mode
	52	Dump mode
	53	Idle mode
	54,55	Rgtr sel (A,P,Q,K)
7	56	Clock wide
	57	Clock narrow
	58	Enbl deadstart/dump/idle
	59	Enbl test mode
	60	Enbl OS bounds checking
	61	Enbl (R) + (A) to PP mem
	62	Individual chan MC
	63	Enbl error stop

IOU 960 (NIO), 962 (CIO) S Register (40)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-37	(Not used)
4-6	38-55	Int rgtr (A,P,Q,K)
7	56	LDS bit
	57	Timing margin (fast)
	58	Timing margin (slow)
	59,60	PP barrel reconfiguration (not used on 962)
	61-63	PP reconfiguration

IOU 960 (NIO), 962 (CIO) FS1 Register (80)

Byte	Bit(s)	Description
0	00-02	(Not used)
	03-07	BAS 0 PP 4-0 error
1	08-10	(Not used)
	11-15	BAS 1 PP 4-0 error
2	16-18	(Not used)
	19-23	BAS 2 PP 4-0 error
3	24-26	(Not used)
	27-31	BAS 3 PP 4-0 error
4	32	Error detected on JW (960) or HW (962) module
	33	Error detected on KR module
	34	Error detected on JA (960) or HA (962) module
	35	Error detected on KB module
	36	Error detected on JC/JU (960) or HC (962) module
	37	Error detected on JD (960) or HT (962) module
	38	Error detected on JE/JV module
	39	Error detected on JF module
5	40-43	SECDDED error BAS 0-3
	44	12/16 conversion error
	45	OS bounds violation
	46	OS boundary adrs PE
	47	Firmware error
6	48	Response code error
	49	Uncorrected CM read error
	50	Uncorrected CM write error
	51	CM reject
	52	Data in error - CMI/ADU
	53	Tag in error - CMI/ADU
	54	Data out error - CMI/ADU
	55	Address/function error - CMI/ADU/BAS
7	56	Tag out error - CMI/ADU
	57	CMI error - JJ module at AO6 (960) or HJ module at B22/D22 (962)
	58	CMI error - JJ module at AO7 (960) or HJ module at B28/D28 (962)
	59	CMI error - JG module at A08 (960) or HG module at B25/D25 (962)
	60	CMI error - JH module at A02 (960) or HH module at B23/D23 (962)
	61	CMI error - JH module at A03 (960) or HH module at B24/D24 (962)
	62	CMI error - JH module at A04 (960) or HH module at B26/D26 (962)
	63	CMI error - JH module at A05 (960) or HH module at B27/D27 (962)

IOU 960 (NIO), 962 (CIO) FS2 Register (81)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	Error, channel 7-0
5	40	Error, channel 17
	41	(Not used)
	42	Error, channel 15
	43	(Not used)
	44-47	Error, channel 13-10
6	48-55	Error, channel 27-20
7	56	MAC error
	57,58	(Not used)
	59	Error, radial interface 1/2/3
	60-63	Error, channel 33-30

IOU 960 (NIO), 962 (CIO) TM Register (A0)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-47	(Not used)
6	48-50	(Not used)
	51,52	Logical barrel number
	53-55	Logical PP number
7	56,57	(Not used)
	58-63	Test code

NOTE

Test codes 00-27 apply to barrels 0-3.

Test Code	Function
00	(Not used)
01	Invert chan to PP parity at generator
02	Invert PP to chan parity at generator
03	Invert PPM to R rgtr parity at generator
04	Invert PPM parity at checker
05	Invert microcode data parity at checker
06	Invert PPM parity at generator
07	Invert CM fctn code parity at generator
10	Invert Y rgtr parity at generator
11	Invert A rgtr parity at generator
12	Invert shift control ROM parity at checker
13	Invert Q rgtr parity at generator
14	Invert P rgtr parity at generator
15	Invert G rgtr parity at generator
16	Invert R to Y parity at generator
17	Invert PPM adrs parity at checker
20	Invert tag out parity at generator (ADU) JE module
21	Invert data-in parity at generator (ADU) JF module
22	Invert central mem adrs
23	Invert SECDED code to PP mem
24-27	(Not used)

NOTE

Test codes 30-37 apply to CMI.

Test Code	Function
30	Force CM request priority/resynch error
31	Force tag in PE
32	Force tag out PE
33	Force response code PE
34	Invert fctn out parity bit
35	Force adrs out parity bit low
36	Force data in parity bit low
37	Force data out parity bit low

NOTE

Test codes 40-47 apply to MAC.

Test Code	Function
40	Invert chan parity
41	Invert MR write parity
42	Invert nanocode parity
43	Invert read parity bit
44	Invert chan 15 data bus parity at checker
45	Invert R/I read data parity
46	Invert R/I read data parity
47	(Not used)

NOTE

Test codes 50-57 apply to ADU/CMI.

Test Code	Function
50	Force CM request (ADU) JD (960) or HT (962) module
51	Force tag in PE (ADU) JD (960) or HT (962) module
52	Force response code PE (ADU) JD (960) or HT (962) module
53	Block D5 full (ADU) JD (960) or HT (962) module
54	Force CMC busy at CMI
55	Force OSB adrs PE
56	Set inhibit PP CM request
57	Clear inhibit PP CM request

IOU 960 (CIO) OI Register (16)

Byte	Bit(s)	Description								
0	00-07	(Not used)								
1	08-15	(Not used)								
2	16-21 22,23	(Not used) Barrel 1,0								
3	24-31	Channel 7-0								
4	32 33 34 35-37 38,39	Channel 17 (Not used) Channel 15 (Not used) Channel 11,10								
5	40-47	(Not used)								
6	48-51	Channel code bits 0-3								
		<table><tr><th>Code</th><th>Type</th></tr><tr><td>03</td><td>ISI</td></tr><tr><td>05</td><td>170</td></tr><tr><td>07</td><td>IPI</td></tr></table>	Code	Type	03	ISI	05	170	07	IPI
Code	Type									
03	ISI									
05	170									
07	IPI									
7	52-55	(Not used)								
	56-63	(Not used)								

IOU 960 (CIO) FSM Register (1C)

Byte	Bit(s)	Description
0	00-02 03-07	(Not used) Mask vector, barrel 0 PP4-0
1	08-10 11-15	(Not used) Mask vector, barrel 1 PP4-0
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	Mask vector, channel 7-0
5	40-45 46,47	(Not used) Mask vector, channel 11,10
6	48-55	(Not used)
7	56-63	(Not used)

IOU 960 (CIO) OSB Register (25)

Byte	Bit(s)	Description
0	00-02	(Not used)
	03-07	Bit vector, barrel 0 PP4-0
1	08-10	(Not used)
	11-15	Bit vector, barrel 1 PP4-0
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-47	(Not used)
6	48-55	(Not used)
7	56-63	(Not used)

IOU 960 (CIO) EC Register (34)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32	Constant one
	33-35	(Not used)
	36-39	PP number
5	40-43	(Not used)
	44-47	Channel number
6	48-50	(Not used)
	51	Load mode
	52	Dump mode
	53	Idle mode
	54,55	Rgtr sel (A,P,Q,K)
7	56,57	(Not used)
	58	Enbl deadstart/dump/idle
	59	Enbl test mode
	60	Enbl OS bounds checking
	61	Enbl (R)+(A) to PP mem
	62	Individual chan MC
	63	Enbl error stop

IOU 960 (CIO) S Register (44)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-37	(Not used)
4-6	38-55	Int rgtr (A,P,Q, or K)
7	56-63	(Not used)

IOU 960 (CIO) FS1 Register (84)

Byte	Bit(s)	Description
0	00-02	(Not used)
	03-07	BAS 0 PP 4-0 error
1	08-10	(Not used)
	11-15	BAS 1 PP 4-0 error
2	16-23	(Not used)
3	24-31	(Not used)
4	32	Error detected on JW module
	33	Error detected on KR module
	34	(Not used)
	35	Error detected on KB module
	36	Error detected on JC/JU module
	37	Error detected on JD module
	38	Error detected on JE/JV module
	39	Error detected on JF module
5	40,41	SECEDED error BAS 0,1
	42,43	(Not used)
	44	12/16 conversion error
	45	OS bounds violation
	46	OS boundary adrs PE
	47	Firmware error
6	48	Response code error
	49	Uncorrected CM read error
	50	Uncorrected CM write error
	51	CM reject
	52	Data in error - CMI/ADU
	53	(Not used)
	54	Data out error - CMI/ADU
	55	Address/function error - CMI/ADU/BAS
7	56-63	(Not used)

IOU 960 (CIO) FS2 Register (85)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	Error, channel 7-0
5	40-45	(Not used)
	46,47	Error, channel 11,10
6	48-55	(Not used)
7	56-63	(Not used)

IOU 960 (CIO) TM Register (A4)

Byte	Bit(s)	Description
0	00-07	(Not used)
1	08-15	(Not used)
2	16-23	(Not used)
3	24-31	(Not used)
4	32-39	(Not used)
5	40-47	(Not used)
6	48-50	(Not used)
	51,52	Logical barrel number
	53-55	Logical PP number
7	56,57	(Not used)
	58-63	Test code

NOTE

Test codes 00 through 27 apply to barrels 0 through 3.

Test Code	Function
00	(Not used)
01	Invert chan to PP parity at generator
02	Invert PP to chan parity at generator
03	Invert PPM to rgtr parity at generator
04	Invert PPM parity at checker
05	Invert microcode data parity at checker
06	Invert PPM parity at generator
07	Invert CM fctn code parity at generator
10	Invert Y rgtr parity at generator
11	Invert A rgtr parity at generator
12	Invert shift control ROM parity at checker
13	Invert Q rgtr parity at generator
14	Invert P rgtr parity at generator
15	Invert G rgtr parity at generator
16	Invert R to Y parity at generator
17	Invert PPM adrs parity at checker
20	Invert tag out parity at generator (ADU) JE module
21	Invert data-in parity at generator (ADU) JF module
22	Invert central mem adrs
23	Invert SECDED code to PP mem
24-27	(Not used)

IOU 960 (CIO), 962 Channels 0 - 11 S Registers (B0 - B9), IOU 962 Channels 20 - 31 S Registers (C0 - C9)**ISI Channel Adapter**

Byte(s)	Bit(s)	Description
0	00,01	(Not used)
	02	Uncorrected CM error
	03	CM reject
	04	Invalid CM response
	05	Response code PE
	06	CMI read data PE
	07	TM compare error
1	08	Overflow error
	09	ISI input
	10	ISI timeout
	11	JY data error
	12	BAS PE
	13	JZ error
	14	JY error
2	15	JX error
	16-23	(Not used)
3	24	(Not used)
	25	Input bfr full
	26	Pause
	27	Sync in
	28	Sync out
	29	Command sequence
	30	Select active
	31	Select hold

NOTE

For 962 channels 0 and 1 S register (B0 and B1), bits 44-47 are the only bits used.

Byte(s)	Bit(s)	Description
4	32	(Not used)
	33	Echo mode
	34	Output mode
	35	PP mode
	36	DMA mode
	37	Non-interlocked mode
	38	T rgtr empty
	39	Transfer in progress
5	40-43	(Not used)
	44	Active flag
	45	Full flag
	46	Error flag
	47	Chan flag
6	48	Enbl cache invalidate
	49	Port B enbl
	50	Dsbl ISI
	51	Enbl test mode
	52	Inhibit TM incr
	53	Inhibit sync out
	54	Inhibit out request cntr
7	55	Enbl idle mode
	56	Enbl force error codes
	57,58	(Not used)
	59	Force error 0
	60	Force error 1
	61	Force error 2
	62	Force error 3
	63	Force error 4

To present the information in this chapter in a structured format, this page has been left blank.

170 Channel Adapter

Byte(s)	Bit(s)	Description
0	00,01	(Not used)
	02	Uncorrected CM Error
	03	CM reject
	04	Invalid response
	05	Any response code PE
	06	CMI read data PE
	07	Clock fault
1	08	Overflow error
	09	Input data error
	10	12/16 conversion error
	11	A/D data error
	12	BAS PE
	13	KZ board error
	14	JY board error
2	15	KX board error
	16-23	PP word counter bits 56 through 63
3	24-27	(Not used)
	28	Output buffer full
	29	Input buffer full
	30	Data available to channel
	31	Fast transfer
4	32	External clock present
	33	Test mode
	34	PP word count = 0
	35	DMA output
	36	DMA input
	37	DMA halted
	38	T register empty
5	39	Transfer in progress
	40,41	(Not used)
	42	Full I
	43	Full II
	44	Active
	45	Full I or Full II
	46	Error flag
6	47	Channel flag
	48	Enable cache invalidate
	49	(Not used)
	50	60-bit mode
	51	Enable test clock
	52	Disable external clock
	53	Block full out
7	54	Enable overflow
	55	Disable error register clear
	56	Enable force error codes
	57,58	(Not used)
	60-63	Force error code bits 0 through 4

IPI Channel Adapter

Byte(s)	Bit(s)	Description
0	00	(Not used)
	01	Illegal function or sequence
	02	Uncorrected CM Error
	03	CM reject
	04	Invalid response code
	05	CM response code PE
	06	CMI read data PE
	07	IPI error
1	08	DMA register PE
	09	MAC status PE
	10	Timeout
	11	A/D data error
	12	BAS reject PE
	13	LZ board error
	14	JY board error
	15	LX board error
2	16	Buffer count PE
	17	(Not used)
	18	Sync count PE
	19	Period count PE
	20	Function upper PE
	21	Function lower PE
	22,23	(Not used)
3	24	Lost data
	25	ICI upper data PE
	26	ICI lower data PE
	27	IPI sequence error
	28	IPI bus A PE
	29	IPI bus B PE
	30	Illegal operation
	31	(Not used)
4	32,33	(Not used)
	34	Output mode
	35	(Not used)
	36	DMA/IPI mode
	37	DMA/IPI inactive
	38	T prime register empty
	39	Transfer in progress

Byte(s)	Bit(s)	Description
5	40-43	(Not used)
	44	Active
	45	Full
	46	Error
	47	Flag
6	48	Enable cache invalidate
	49	(Not used)
	50	Disable timeout
	51	Enable test mode
	52	Inhibit test mode increment
	53	Enable transfer in progress flag
	54	Enable T prime empty flag
7	55	(Not used)
	56	Error
	57	Attention
	58	Buffer not empty
	59	Select out
	60	Slave in
	61	Master out
	62	Sync in
	63	Sync out

IOU Error Isolation

Two methods exist for isolating errors in the IOU. One involves using the light-emitting diodes (LEDs) on the logic modules. The other requires interpreting error information stored in the fault status registers.

Approximately 80 percent of the IOU modules have LEDs that light when that module detects an error. Once lit, an error-detecting LED remains lit until the IOU MAC performs the clear LED function. These LEDs point to the most likely source of the failure and identify the first module to replace.

Isolating errors with fault status 1 (FS1) and fault status 2 (FS2) maintenance registers is more involved. However, with this method, second and third probable causes of the failure are identified. Before using these procedures, check bit 61 of the status summary register. If set, determine if any FS1 bits are set. If no FS1 bits are set, check the FS2 bits. If any FS1 or FS2 bits are set, use the corresponding fault isolation procedure.

FS1 Register Fault Isolation

The matrix shown in figure B-1 can be used to isolate the source of a failure indicated by bits set in FS1 register 80 (960 NIO and 962) or 84 (960 CIO).

Errors are valid when any of bits 32 through 63 of the FS1 register are set to intersect at numbered positions in the matrix. The x positions provide further error information. If an error is valid, the x positions are always accompanied by an intersecting numbered position.

Use the following procedure to isolate an error with the FS1 register.

1. Examine FS1 register for set bits.
2. Indicate on FS1 register matrix below which of bits 32 through 63 are set.
3. Determine if set bits intersect on a numbered position in the matrix. If set bits do not intersect on a number, call CHS. If bits do intersect on a number, go to step 4.
4. Perform the corrective action (see table B-1) associated with the number in the matrix. If more than one action is listed under the same number in the table, the actions listed first should be performed first.

[illegible]

NOTE:

† NOT USED IN FS1 REGISTER 84 (960 CIO).

M02922

Figure B-1. FS1 Register Bit Matrix

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Table B-1. Corrective Actions for FS1 Matrix

Matrix Number	Sequence Number	Corrective Action
1	1	Replace module number 01 of table B-2. Conversion error occurred during a channel input.
	2	Replace the channel module for the channel being operated on.
	3	Because the channel data is on a data bus, any of the channel modules on that bus (CQ at B22, JL at B02-B07 or B16-B21, JM at B01) could have caused the error.
2	1	Replace module number 01 of table B-2.
	2	Replace module number 04 of table B-2.
	3	Replace module number 02 of table B-2.
3	1	Replace module number 01 of table B-2.
	2	Replace the channel module of the channel being operated on.
	3	Because the channel data is on a data bus any of the channel modules on that bus (CQ at B22, JL at B02-B07 or B16-B21, JM at B01) could cause the error.
4	1	Replace module number 02 of table B-2.
	2	Replace module number 04 of table B-2.
	3	Replace module number 01 of table B-2.
5	1	Replace module number 03 of table B-2.
	2	Other possible causes could be a module in the memory element or a cable problem.
6	1	Replace module number 04 of table B-2.
	2	Replace module number 01 of table B-2.
	3	Replace module number 01 of table B-2.
	4	Replace module number 08 of table B-2.
	5	Replace module number 05 of table B-2.
7	1	Replace module number 05 of table B-2.
	2	Replace MAC JQ module at location A22 (960) or HQ module at location B01 (962).

(Continued)

Table B-1. Corrective Actions for FS1 Matrix *(Continued)*

Matrix Number	Sequence Number	Corrective Action										
8	1	Replace module number 05 of table B-2.										
	2	Replace module number 02 of table B-2.										
	3	Replace module number 06 of table B-2.										
9	1	Replace module number 05 of table B-2.										
	2	Replace module number 02 of table B-2.										
	3	Replace MRB JT module at location A21 (960) or HT module at location A21/C21 (962).										
10	1	Replace module number 06 of table B-2.										
	2	Replace module number 13 of table B-2.										
11	1	Replace module number 06 of table B-2.										
	2	Replace module number 15 of table B-2.										
12	1	Replace module number 06 of table B-2.										
13	1	Replace module number 07 of table B-2.										
	2	Replace module number 04 of table B-2.										
14	1	Replace module number 07 of table B-2.										
	2	Replace module number 01 of table B-2.										
15	1	Replace module number 07 of table B-2.										
16	1	Replace module number 08 of table B-2.										
	2	The error could be caused by modules 16 through 19 of table B-2. If the failing bit is known, replace one of the following modules.										
		<table><tr><th>Failing Bit</th><th>Replace</th></tr><tr><td>0-15</td><td>Module 16 of table B-2.</td></tr><tr><td>16-31</td><td>Module 17 of table B-2.</td></tr><tr><td>32-47</td><td>Module 18 of table B-2.</td></tr><tr><td>48-63</td><td>Module 19 of table B-2.</td></tr></table>	Failing Bit	Replace	0-15	Module 16 of table B-2.	16-31	Module 17 of table B-2.	32-47	Module 18 of table B-2.	48-63	Module 19 of table B-2.
Failing Bit	Replace											
0-15	Module 16 of table B-2.											
16-31	Module 17 of table B-2.											
32-47	Module 18 of table B-2.											
48-63	Module 19 of table B-2.											
17	1	Replace module number 09 of table B-2.										
18	1	Replace module number 10 of table B-2.										

(Continued)

Table B-1. Corrective Actions for FS1 Matrix *(Continued)*

Matrix Number	Sequence Number	Corrective Action
19	1	Replace module number 11 of table B-2.
20	1	Replace module number 12 of table B-2.
21	1	Replace module number 13 of table B-2.
	2	The error could be caused by a defective module in CMC. Refer to CP panel map shown in figure F-5.
22	1	Replace module number 13 of table B-2.
	2	If bit 49 or 50 of FS1 is set, replace module number 05 of table B-2.
		If bit 51 of FS1 is set, replace module number 07 of table B-2.
		If channel bit is set in FS2 register, refer to FS2 error isolation procedure.
	3	Because the address and function are on a data bus, any location listed in module numbers 5 or 7 of table B-2 could cause the error.
23	1	Replace module number 14 of table B-2.
	2	If bit 49 or 50 of FS1 is set, replace module number 05 of table B-2.
		If a channel bit is set in the FS2 register, refer to FS2 error isolation procedure.
	3	Because the address is on a data bus, any location listed in module number 05 of table B-2 could cause the error.
24	1	Replace module number 15 of table B-2.
	2	See step 2 of number 21.
25	1	Replace module number 15 of table B-2.
	2	Replace module number 06 of table B-2.
	3	Replace module number 07 of table B-2.
26	1	Replace module number 15 of table B-2.

(Continued)

Table B-1. Corrective Actions for FS1 Matrix *(Continued)*

Matrix Number	Sequence Number	Corrective Action
27	1	Replace module number 16 of table B-2 ¹ .
	2	See step 2 of number 21.
28	1	Replace module number 16 of table B-2.
	2	If bit 49 or 50 of FS1 is set, replace module number 07 of table B-2. If a channel bit is set in the FS2 register, refer to FS2 error isolation procedure.
	3	Because the data is on a data bus, any location listed in module number 07 of table B-2 could cause the error.
29	1	Replace module number 17 of table B-2 ¹ .
	2	See step 2 of number 21.
30	1	Replace module number 17 of table B-2.
	2	See step 2 of number 28.
	3	See step 3 of number 28.
31	1	Replace module number 18 of table B-2.
	2	See step 2 of number 21.
32	1	Replace module number 18 of table B-2.
	2	See step 2 of number 28.
	3	See step 3 of number 28.
33	1	Replace module number 19 of table B-2.
	2	See step 2 of number 21.
34	1	Replace module number 19 of table B-2.
	2	See step 2 of number 28.
	3	See step 3 of number 28.

Note:

1. System will set FS1 bits 52 and 60 through 63 when FS1 bit 49, 50, or 51 sets.

(Continued)

Table B-1. Corrective Actions for FS1 Matrix *(Continued)*

Matrix Number	Sequence Number	Corrective Action
35	1	Replace module number 01 of table B-2. Conversion error occurred during a channel output.
	2	Replace module number 04 of table B-2.
	3	Replace module number 02 of table B-2.
36	1	Check operating system setup to see if this is a valid error. This error may occur because of the software and may be expected.
	2	If not expected, replace module number 05 of table B-2.
	3	If not expected, replace module number 07 of table B-2.
37		These errors are not detected by the IOU. The error status is a decode of the response code received from CMC.

Table B-2 shows chassis locations for the modules recommended for replacement in table B-1. For module numbers next to more than one location, determine which location applies by checking the appropriate FS1 register to see which barrel number has a bit set in it. Then select the location from the column for that barrel in table B-2.

Table B-2. Module Number/Chassis Location Correlation

Module Number	Location	BAS 0	BAS 1	BAS 2	BAS 3
960 NIO					
01	A01	B14	B12	B10	B08
02		B15	B13	B11	B09
03					
04		B28	B27	B26	B25
05		A11	A11	A10	A10
06		A15	A15	A15	A15
07		A14	A14	A13	A13
08		A18	A18	A17	A17
09	B28				
10	B27				
11	B26				
12	B25				
13		A06	A06	A06	A06
14		A07	A07	A07	A07
15		A08	A08	A08	A08
16		A02	A02	A02	A02
17		A03	A03	A03	A03
18		A04	A04	A04	A04
19		A05	A05	A05	A05
960 CIO					
01	A01	D24	C24		
02		D25	C25		
03					
04		D26	C26		
05		A09	A09		
06		A15	A15		
07		A12	A12		
08		A16	A16		
09	B28				
10	B27				
11	B26				
12	B25				
13		A06	A06		
14		A07	A07		
15		A08	A08		
16		A02	A02		
17		A03	A03		
18		A04	A04		
19		A05	A05		

(Continued)

Table B-2. Module Number/Chassis Location Correlation *(Continued)*

Module Number	Location	BAS 0	BAS 1	BAS 2	BAS 3
962					
01	A20	B15	A17	D17	C17
02		B16	A18	D18	C18
03					
04		B17	A19	D19	C19
05		A24	A24	D24	D24
06		A21	A21	D21	D21
07		A22	A22	D22	D22
08		A23	A23	D23	D23
09	B17				
10	A19				
11	C19				
12	D19				
13		B22	B22	D22	D22
14		B28	B28	D28	D28
15		B25	B25	D25	D25
16		B23	B23	D23	D23
17		B24	B24	D24	D24
18		B26	B26	D26	D26
19		B27	B27	D27	D27

FS2 Register Fault Isolation (960)

The following information describes how to use the FS2 registers to isolate failures. The FS2 register for the NIO is interpreted differently than the FS2 register for the CIO.

NIO FS2 Register Errors

Bits set in the NIO FS2 register can be used to isolate a failure to the highest probable field-replaceable unit. Examine the register for set bits. If any of bits 32 through 63 are set, perform the suggested corrective action described in following tables. Table B-3 provides corrective actions if bits 32 through 39, 44 through 55, or 60 through 63 are set. Table B-4 describes what action to take if any of bits 40, 42, 56, 58, or 59 are set.

Table B-3. NIO FS2 Corrective Actions I

NIO FS2	
Bits Set	First Corrective Action
32 or 33	Replace module JL at location B18.
34 or 35	Replace module JL at location B19.
36 or 37	Replace module JL at location B20.
38 or 39	Replace module JL at location B21.
44 or 45	Replace module JL at location B16.
46	Replace module JL at location B17.
47	Replace module CQ at location B22.
48 or 49	Replace module JL at location B04.
50 or 51	Replace module JL at location B05.
52 or 53	Replace module JL at location B06.
54 or 55	Replace module JL at location B07.
60 or 61	Replace module JL at location B02.
62 or 63	Replace module JL at location B03.
NIO FS2	
Bits Set	Second Corrective Action
Any bits from above	The peripheral equipment connected to the channel with the failure is itself failing. Attach peripheral to a channel known to be good to verify the condition of the peripheral equipment.
NIO FS2	
Bits Set	Third Corrective Action
Any bits from above	Replace the JW module associated with the failing channel.

Table B-4. NIO FS2 Corrective Actions II

NIO FS2 Bit Set	Sequence Number	Corrective Action
40	1	Replace module JM at location B01.
	2	Replace module JQ at location A22.
	3	Replace module JR at location A23 if FS2 bit 59 is set.
42	1	Replace module JM at location B01.
	2	Replace module JK at location B23.
	3	Replace module JW module for the PP that was outputting to channel 15.
56	1	Replace module JQ at location A22.
	2	Replace module JM at location B01.
	3	Replace module JK at location B23.
59	1	Replace module JR at location A23.
	2	Replace module JQ at location A22.
	3	System element connected to radial interfaces 1, 2, or 3.

CIO FS2 Register Errors

Ten channel error bits in the 64-bit CIO FS2 register (address 8516) indicate which CIO channel adapter experienced an error. Channel error bits 32 through 39 point (when set) to channels 7 through 08. Channel error bits 46 and 47 point (when set) to channels 11 and 108.

Channel Status Registers

There is one 64-bit channel status register for each CIO channel. The channel status register contains a number of registers, including an error status register (ISI, CY170, IPI) and an error register (IPI only).

Use the following procedure to isolate an error in a channel adapter:

1. Check CIO Register Data on the system console screen. Examine the ten CIO FS2 register channel error bits (bytes 4 and 5, bits 32-39 and 46, 47) to determine the failing channel number.
2. Check CIO Register Data on the system console screen. Examine the error status register (bytes 0 and 1, bits 0-15) or the IPI error register (bytes 2 and 3, bits 16-31) associated with the failing channel.
3. See figure B-2 (error status register) or figure B-3 (IPI error register) for the correlation between the registers' bit locations within the channel status register and the level 4 diagrams.

Note which bits were set in step 2. Plot the bits on the module isolation matrix shown in figure B-4 (ISI, CY170) or in figures B-5 through B-7 (IPI).

4. Determine if valid error(s) occurred by observing if bits set on the X and Y coordinates of the matrix intersect at a matrix number. If they do, the error(s) is valid and you should proceed to step 5. If not, contact the next level of support.

5. The matrix number from a valid error will point to a corrective action listed in table B-5 (ISI, CY170) or B-6 (IPI). The actions are listed in sequence, with the most probable one first.

BYTE 0								BYTE 1							
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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NOTES:

1. THE LOWER ROW OF BIT NUMBERS (0 THROUGH 15) ARE THE ACTUAL ERROR STATUS REGISTER BIT LOCATIONS WITHIN THE 64-BIT CIO CHANNEL STATUS REGISTER.
2. THE UPPER ROW OF BIT NUMBERS (48 THROUGH 63) ARE THE ERROR STATUS REGISTER BIT LOCATIONS IN THE LEVEL 4 DIAGRAM.

Figure B-2. Error Status Register to Level 4 Diagram Bit Correlation-ISI, CY170, IPI

BYTE 2								BYTE 3							
56	57	58	59	60	61	62	63	56	57	58	59	60	61	62	63
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

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NOTES:

1. THE LOWER ROW OF BIT NUMBERS (16 THROUGH 31) ARE THE ACTUAL IPI ERROR REGISTER BIT LOCATIONS WITHIN THE 64-BIT CIO CHANNEL STATUS REGISTER.
2. THE UPPER ROW OF BIT NUMBERS (56 THROUGH 63) ARE THE IPI ERROR REGISTER BIT LOCATIONS IN THE LEVEL 4 DIAGRAM.

Figure B-3. IPI Error Register to Level 4 Diagram Bit Correlation

CIO Module Isolation Matrix - ISI

The matrix shown in figure B-4 is used to isolate an error within a DMA enhanced ISI channel adapter. Review the error isolation procedure located under CIO FS2 Register Errors before using the isolation matrix. Refer to table B-5 for corrective actions.

MATRIX NUMBER												
JZ ERROR 61							1	1				2
JY ERROR 62										3		4
JX ERROR 63				5							6	7
BITS 61, 62, 63 CLEAR	8	8	5	9	10	11			1			
	50	51	52	53	54	55	56	57	58	59	60	
UNCORRECTED CM ERROR												
CM REJECT												
INVALID CM RESPONSE												
RESPONSE CODE PARITY ERROR												
CMI READ DATA PARITY ERROR												
TEST MODE ERROR												
OVERFLOW ERROR												
INPUT ERROR												
TIMEOUT												
JY DATA ERROR												
BAS PARITY ERROR												
BITS 50-60 CLEAR												

NOTE: BITS 48 AND 49 ARE NOT USED.

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Figure B-4. CIO Module Isolation Matrix - ISI Status Register Bits

Table B-5. Corrective Actions for CIO Module Isolation Matrix - ISI

Matrix Number	Sequence Number	Corrective Action										
1	1	Replace JZ for the failing channel.										
	2	Replace JX for the failing channel.										
	3	Failure in I/O cables or external device.										
2	1	Replace JZ for the failing channel.										
	2	Replace JX for the failing channel.										
	3	Replace JY for the failing channel.										
3	1	Replace JY for the failing channel.										
	2	Replace JZ for the failing channel.										
	3	Other causes of this error could be the CMI data modules. If the failing bit is known, replace the failing module as follows:										
		<table><tr><th>Failing Bit</th><th>Replace</th></tr><tr><td>0-15</td><td>Module JH (location A02).</td></tr><tr><td>16-31</td><td>Module JH (location A03).</td></tr><tr><td>32-47</td><td>Module JH (location A04).</td></tr><tr><td>48-63</td><td>Module JH (location A05).</td></tr></table>	Failing Bit	Replace	0-15	Module JH (location A02).	16-31	Module JH (location A03).	32-47	Module JH (location A04).	48-63	Module JH (location A05).
Failing Bit	Replace											
0-15	Module JH (location A02).											
16-31	Module JH (location A03).											
32-47	Module JH (location A04).											
48-63	Module JH (location A05).											
4	1	Replace JY for the failing channel.										
	2	Replace JX for the failing channel.										
5	1	Replace JX for the failing channel.										
	2	Replace JJ (location A06).										
	3	The response code is on a bus, therefore the failure could be in any module on the bus.										

(Continued)

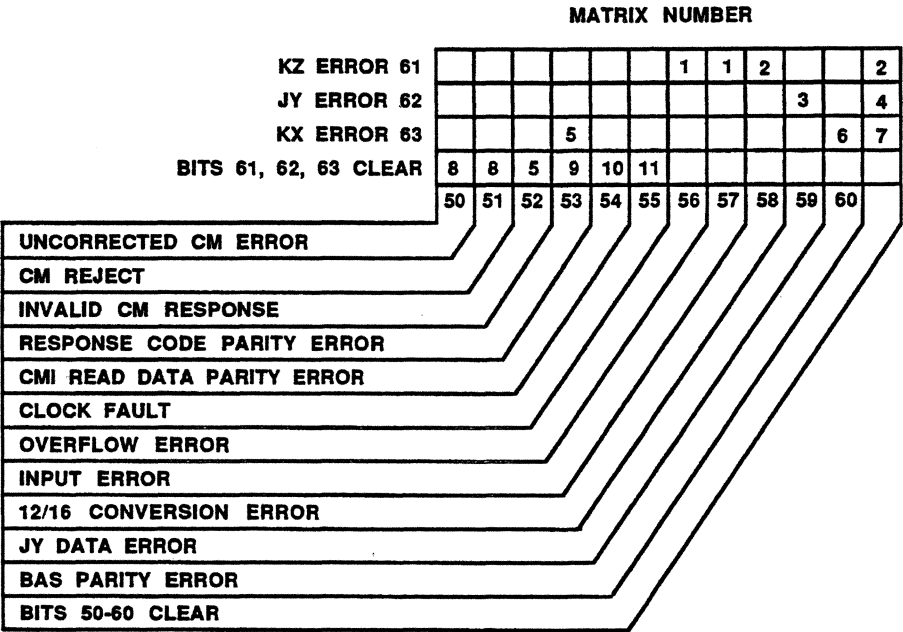
Table B-5. Corrective Actions for CIO Module Isolation Matrix - ISI (Continued)

Matrix Number	Sequence Number	Corrective Action
6	1	Replace JX for the failing channel.
	2	Error in channels 00-04, replace JW (location D24). Error in channels 05-11, replace JW (location C24).
	3	The channel data is on a bus, therefore any bad JX module on the bus could cause the error.
7	1	Replace JX for the failing channel.
	2	Replace JZ for the failing channel.
	3	Replace JY for the failing channel.
8		These errors are not detected by the IOU. The error status is a decode of the response received from the memory element.
9	1	Replace JJ (location A06).
	2	Replace JX for the failing channel.
	3	Another possible cause of the error could be a defective module in the memory element.
10		This error should be isolated via the NIO fault status 1 (FS1) register. The error is only repeated in the error status register so the PP can determine if the transfer completed correctly.
11	1	Replace JZ for failing channel.
	2	Replace JY for failing channel.
	3	Replace JX for the failing channel.

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CIO Module Isolation Matrix - CY170

The matrix shown in figure B-5 is used to isolate an error within a DMA enhanced CY170 channel adapter. Review the error isolation procedure located under CIO FS2 Register Errors before using the isolation matrix. Refer to table B-6 for corrective actions.



NOTE: BITS 48 AND 49 ARE NOT USED. M02924

Figure B-5. CIO Module Isolation Matrix - CY170 Error Status Register Bits

Table B-6. Corrective Actions for CIO Module Isolation Matrix - CY170

Matrix Number	Sequence Number	Corrective Action										
1	1	Replace KZ for the failing channel.										
	2	Replace KX for the failing channel.										
	3	Failure in I/O cables or external device.										
2	1	Replace KZ for the failing channel.										
	2	Replace KX for the failing channel.										
	3	Replace JY for the failing channel.										
3	1	Replace JY for the failing channel.										
	2	Replace KZ for the failing channel.										
	3	Other causes of this error could be the CMI data modules. If the failing bit is known, replace the failing module as follows:										
		<table><tr><th>Failing Bit</th><th>Replace</th></tr><tr><td>0-15</td><td>Module JH (location A02).</td></tr><tr><td>16-31</td><td>Module JH (location A03).</td></tr><tr><td>32-47</td><td>Module JH (location A04).</td></tr><tr><td>48-63</td><td>Module JH (location A05).</td></tr></table>	Failing Bit	Replace	0-15	Module JH (location A02).	16-31	Module JH (location A03).	32-47	Module JH (location A04).	48-63	Module JH (location A05).
Failing Bit	Replace											
0-15	Module JH (location A02).											
16-31	Module JH (location A03).											
32-47	Module JH (location A04).											
48-63	Module JH (location A05).											
4	1	Replace JY for the failing channel.										
	2	Replace KX for the failing channel.										
5	1	Replace KX for the failing channel.										
	2	Replace JJ (location A06).										
	3	The response code is on a bus, therefore the failure could be in any module on the bus.										

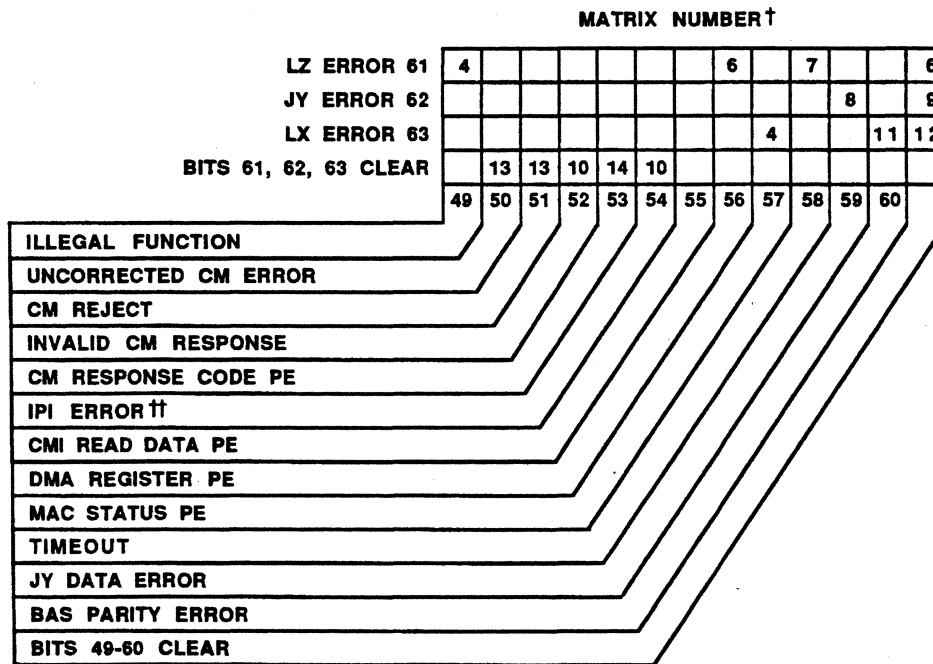
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Table B-6. Corrective Actions for CIO Module Isolation Matrix - CY170
(Continued)

Matrix Number	Sequence Number	Corrective Action
6	1	Replace KX for the failing channel.
	2	Error in channels 00-04, replace JW (location D24). Error in channels 05-11, replace JW (location C24).
	3	The channel data is on a bus, therefore any bad KX module on the bus could cause the error.
7	1	Replace KX for the failing channel.
	2	Replace KZ for the failing channel.
	3	Replace JY for the failing channel.
8		These errors are not detected by the IOU. The error status is a decode of the response received from the memory element.
9	1	Replace JJ (location A06).
	2	Replace KX for the failing channel.
	3	Another possible cause of the error could be a defective module in the memory element.
10		This error should be isolated via the NIO fault status 1 (FS1) register. The error is only repeated in the error status register so the PP can determine if the transfer completed correctly.
11	1	Switch changed in the ESM II.
	2	Fault in ESM II.
	3	Replace KZ for failing channel.

CIO Module Isolation Matrixes - IPI

The matrixes shown in figure B-6 (error status register) and figures B-7 and B-8 (IPI error register) are used to isolate an error in the DMA enhanced IPI channel adapter. Review the error isolation procedure located under CIO FS2 Register Errors before using the isolation matrixes. Refer to table B-7 for corrective actions.



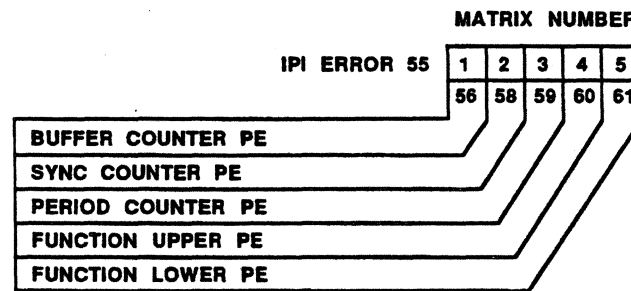
M02925

NOTES:

† BIT 48 IS NOT USED.

†† IF BIT 55 IS SET, REFER TO FIGURES B-7 AND B-8.

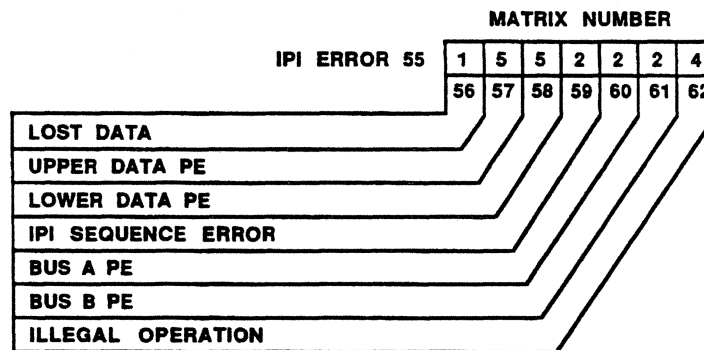
Figure B-6. CIO Module Isolation Matrix - IPI Error Status Register Bits



NOTE: BITS 57, 62, AND 63 ARE NOT USED.

M02926

Figure B-7. CIO Module Isolation Matrix - IPI Error Register Bits (Byte 2)



NOTE: BIT 63 IS NOT USED.

M02927

Figure B-8. CIO Module Isolation Matrix - IPI Error Register Bits (Byte 3)

Table B-7. Corrective Actions for CIO Module Isolation Matrixes - IPI

Matrix Number	Sequence Number	Corrective Action										
1	1	Replace LZ for the failing channel.										
	2	Replace JY for the failing channel.										
	3	Failure in I/O cables or external device.										
2	1	Replace LZ for the failing channel.										
	2	Failure in I/O cables or external device.										
3	1	Replace LZ for the failing channel.										
4	1	Replace LZ for the failing channel.										
	2	Replace LX for the failing channel.										
5	1	Replace LZ for the failing channel.										
	2	Replace JY for the failing channel.										
	3	Replace LX for the failing channel.										
6	1	Replace LZ for the failing channel.										
	2	Replace LX for the failing channel.										
	3	Replace JY for the failing channel.										
7	1	Replace LZ for the failing channel.										
	2	Replace LX for the failing channel.										
	3	Failure in I/O cables or external device.										
8	1	Replace JY for the failing channel.										
	2	Replace LZ for the failing channel.										
	3	Other causes of this error could be the CMI data modules. If the failing bit is known, replace the failing module as follows:										
		<table><tr><th>Failing Bit</th><th>Replace</th></tr><tr><td>0-15</td><td>Module JH (location A02).</td></tr><tr><td>16-31</td><td>Module JH (location A03).</td></tr><tr><td>32-47</td><td>Module JH (location A04).</td></tr><tr><td>48-63</td><td>Module JH (location A05).</td></tr></table>	Failing Bit	Replace	0-15	Module JH (location A02).	16-31	Module JH (location A03).	32-47	Module JH (location A04).	48-63	Module JH (location A05).
Failing Bit	Replace											
0-15	Module JH (location A02).											
16-31	Module JH (location A03).											
32-47	Module JH (location A04).											
48-63	Module JH (location A05).											
9	1	Replace JY for the failing channel.										
	2	Replace LZ for the failing channel.										

(Continued)

Table B-7. Corrective Actions for CIO Module Isolation Matrixes - IPI
(Continued)

Matrix Number	Sequence Number	Corrective Action
10	1	Replace LX for the failing channel.
	2	Replace JJ at A06.
	3	The response code is on a bus, therefore, the failure could be in any module on the bus.
11	1	Replace LX for the failing channel.
	2	Replace JW at D24 if the error is in channels 0-4, or JW at C24 if the error is in channels 5-11.
	3	Because the channel data is on a bus, any of the LX boards on that bus could cause the error.
12	1	Replace LX for the failing channel.
	2	Replace LZ for the failing channel.
	3	Replace JY for the failing channel.
13	1	These errors are not detected by the IOU. The error status is a decode of the response received from the memory element.
14	1	Replace JJ at A06.
	2	Replace LX for the failing channel.
	3	Other possible causes of the error could be a defective module in the memory element.

FS2 Register Fault Isolation (962)

The following information describes how to use the FS2 register to isolate 962 IOU failures.

Channel Status Registers

Eighteen channel error bits in the 64-bit FS2 register indicate which channel adapter experienced an error.

Bits	Channels
32-37	7-2
46,47	11,10
48-55	27-20
62,63	31,30

Refer to FS2 Register Fault Isolation (960) matrixes and tables to troubleshoot the 962 channel status registers.

Other FS2 Register Errors

Table B-8 lists other errors reported to the 962 FS2 register and corrective actions to be taken.

Table B-8. FS2 Corrective Actions

Matrix Number	Sequence Number	Corrective Action
38,39	1	Replace module HL at location B03.
	2	Replace module HW at location B15.
40	1	Replace module HM at location B02.
	2	Replace module HQ at location B01.
	3	Replace module HR at location B21.
42	1	Replace module HM at location B02.
	2	Replace module JK at location B20.
	3	Replace module HW that was outputting to channel 15.
44,45	1	Replace module HL at location B03.
	2	Replace module HW that was outputting to channel 12 or 13.
56	1	Replace module HQ at location B01.
	2	Replace module HM at location B02.
	3	Replace module JK at location B20.
59	1	Replace module HR at location B21.
	2	Replace module HQ at location B01.
	3	Check MAC from other system elements connected to RI 1/2/3.

IOU Registers 80, 81, 84, 85 Bit Definitions

Detailed definitions of these fault status 1 and 2 (FS1 and FS2) registers are provided in the following paragraphs.

Register	Description
80	960 NIO and 962 FS1
81	960 NIO and 962 FS2
84	960 CIO FS1
85	960 CIO FS2

Fault Status 1 Register (80, 84)

The 64-bit FS1 register reports various error conditions in the IOU. All error conditions are unconditionally decoded into a failing PP number, with the exception of the errors listed below:

- Tag in error (bit 53, FS1)¹
- Channel errors (FS2)
- Tag out error (bit 56, FS1)¹
- Data out error (bit 54, FS1)¹
- Address/function error (bit 55, FS1)¹
- OS boundary address parity error (bit 46, FS1)¹
- Error detected on JA (960) or HA (962) module (bit 34, FS1)
- Error detected on JD (960) or HT (962) module (bit 37, FS1)

The following paragraphs describe the FS1 bits.

Bits 0 through 31--BAS/PP errors

These bits, when set, indicate a logical PP in a physical BAS had an error. Bits 0 through 2, 8 through 10, 16 through 18, and 24 through 26 are not used.

Bits	Error
3-7	BAS 0 PP 4-0 error
11-15	BAS 1 PP 4-0 error
19-23	BAS 2 PP 4-0 error (not in 84)
27-31	BAS 3 PP 4-0 error (not in 84)

Bit 32--Error Detected on JW (960) or HW (962) Module

This bit, when set, indicates a parity error has been detected in the firmware (bit 47) or a parity error has been detected in channel to Y data.

1. At the same time, another bit is also set to indicate either the module on which the error was detected or the type of error.

Bit 33--Error Detected on KR Module

This bit, when set, indicates a parity error has been detected on:

- A register shift control ROM data
- PP memory address bits
- PP memory data out
- A register BAS data at rank 3
- R register BAS data at rank 3
- P register BAS data at rank 3
- Q register BAS data at rank 3

Bit 34--Error Detected on JA (960) or HA (962) Module (not in 84)

This bit, when set, indicates the loss of the system clock.

Bit 35--Error Detected on KB Module

This signal indicates one of the following errors has occurred:

- Y mux input data parity error
- Double SECDDED error on PP memory read
- Parity error on rank 2 write data
- Parity error on PP memory address

Bit 36--Error Detected on JC/JU (960) or HC (962) Module

This signal indicates one of the following errors has occurred:

- CM address parity error
- Parity error on R register data selected to the Y mux

Bit 37--Error Detected on JD (960) or HT (962) Module

This bit, when set, indicates one of the following errors has occurred:

- CM response code parity error, bit 48
- Address counters/D5 full compare error
- Address counters equal error
- Tag in parity error, bit 53 (Because the tag bits are at fault, this error may or may not set bit 37.)

Bit 38--Error Detected on JE/JV (960) or JE (962) Module

This bit, when set, indicates one of the following errors has occurred:

- Data out parity error, bit 54
- Function out error, bit 55
- Tag out parity error bit 56 (Because the tag bits are at fault, this error may or may not set bit 38.)

Bit 39--Error Detected on JF Module

This bit, when set, indicates a CM data in parity error at the ADU (bit 52).

Bits 40 through 43 (80); 40, 41 (84)--SECDED Error BAS 0 through 3

These bits, when set, indicate a single SECDED error has been detected by one or more of the PPs within BAS 0 through 3 (80) or 0, 1 (84). The error location in PP memory will be rewritten with corrected data.

Bit 44--12/16 Conversion Error

This bit, when set, indicates an error on channel conversion data on the JW (960) or HW (962) module. If bit 32 is also set, the error occurred during an output. If bit 32 is clear, the error occurred during an input.

Bit 45--OS Bounds Violation

The presence of this bit indicates a PP has attempted to write or exchange at a CM address outside the region allowed by the OS bounds register. This bit will only set if bit 60 of the environmental control (EC) register is set.

Bit 46--OS Boundary Address Parity Error

This bit will set if a parity error is detected on the operating system (OS) boundary address stored in the IOU maintenance register. This address is the boundary for all PPs in each BAS.

Bit 47--Firmware Error

This bit, when set, indicates a parity error in the control firmware. Parity is checked on all bits of the micrand field. Bits 0 through 48, 59, 60, 71 through 87 are treated as firmware data bits and are checked for correct parity at slot time (rank 4). The branch 1 field (bits 49 through 58) and the branch 2 field (bits 61 through 70) are treated as firmware address bits and are checked one major cycle later at slot time (rank 4). The selected branch is checked for parity before addressing the ROMs. These conditions cause the failing PP to unconditionally halt on the following trip. This bit may also set if the instruction from CM has a parity error. This also causes the PP to unconditionally halt.

Bit 48--Response Code Error

This bit, when set, indicates the ADU or CMI has detected a parity error in the response code from CM. If the ADU senses this error on a read request, the ADU will block the response for that request. Thus the PP that made the request will hang.

Bit 49--Uncorrected CM Read Error

This status is decoded from the CM response code when the ADU receives a response. CM reports this status if it detects:

- Multiple SECDED errors or a read parity error
- A parity error (except on function code or tag in signals)

Bit 50--Uncorrected CM Write Error

This status is decoded from the CM response code when the ADU receives a response. CM reports this status if it detects:

- A parity error (except on function code or tag in signals)
- A bounds fault

Bit 51--CM Reject

This status is decoded from the CM response code when the ADU receives a response. If a reject is received on a CM read request, the ADU blocks the response for that request. Thus the PP that made the request will hang. CM reports this status if it detects:

- A function code parity error
- An illegal function code
- A data in error on an interrupt

Bit 52--Data In Error--CMI/ADU

This bit, when set, indicates a parity error on the CM read data at the output of the CMI or ADU.

Bit 53--Tag In Error--CMI/ADU (not in 84)

This bit, when set, indicates a parity error on the tag bits received from CM. Response is inhibited. If this error is detected by the CMI, the CMI control board indicates an error and sets bit 59 of the FS1 register. If this error is detected by the ADU, the ADU control board indicates an error and sets bit 37 of the FS1 register.

Bit 54--Data Out Error--CMI/ADU

This bit sets if a CM data out parity error is detected at the ADU or CMI.

Bit 55--Address/Function Error--CMI/ADU/BAS

This bit, when set, indicates one of the following errors has occurred:

- Function error ADU
- Address/function error CMI
- Address out error BAS

Bit 56--Tag Out Error--CMI/ADU (not in 84)

This bit, when set, indicates the ADU or CMI has detected a parity error in the tag bits being sent to CM. This error condition cannot be decoded into a failing PP number, since the tags define the number of the PP performing the CM operation.

Bit 57--CMI Error--JJ (960) or HJ (962) Module (not in 84)

This bit, when set, indicates the module at location A06 (960) or B22/D22 (962) has detected an error. Bit 48 (response code error) and/or bit 55 (address/function error) also sets.

Bit 58--CMI Error--JJ (960) or HJ (962) Module (not in 84)

This bit, when set, indicates the module at location A07 (960) or B28/D28 (962) has detected an error. Bit 55 (address/function error) also sets.

Bit 59--CMI Error--JG (960) or HG (962) Module (not in 84)

This bit, when set, indicates the module at location A08 (960) or B25/D25 (962) has detected an error. Bit 53 (tag in error) and/or bit 56 (tag out error), when set, will indicate the type of tag error detected. If neither bit 53 nor bit 56 sets, the error was a priority error or resynch error.

Bits 60 through 63--CMI Error--JH (960) or HH (962) Module (not in 84)

These bits, when set, indicate the corresponding module has detected an error.

Bit	Module Location
60	A02 (960) or B23/D23 (962)
61	A03 (960) or B24/D24 (962)
62	A04 (960) or B26/D26 (962)
63	A05 (960) or B27/D27 (962)

Bit 52 (data in error) and/or bit 54 (data out error) will also set.

Fault Status 2 Register (81, 85)

The 64-bit FS2 register reports channel parity errors. Bits 0 through 31, 57, and 58 are not used.

Each channel has its own bit in the register. Channel parity is checked whenever the channel is full. Data in the channel could be from either a PP or an external device. For CYBER 170 channels, parity checking is disabled if the parity switch for that channel is off. This is a software switch that is selectable only at deadstart time. The channel parity error bits are listed below.

Bit(s)	Channel(s)
32-39	7-0
40	17 (not in 85)
42	15 (not in 85)
44,45	13,12 (not in 85)
46,47	11,10
48-55	27-20 (not in 85)
60-63	33-30 (not in 85)

FS2 also reports errors from MAC and RI. These error bits are listed below.

Bit	Error
56	MAC (not in 85)
59	RI 1/2/3 (not in 85)

CMC Registers A0, A4, A8 Bit Definitions

Detailed definitions of the bits in CMC register A0 (corrected error log), A4 (uncorrectable error log 1), and A8 (uncorrectable error log 2) are provided in the following paragraphs.

Corrected Error Log (CEL/A0)

CMC contains a 64-bit CEL that contains the following information about a corrected error. Bits 2 through 8, 44 through 47, and 56 through 63 are not used.

Bit 0--Valid Bit

This bit, when set, indicates the presence of a valid entry in the log.

Bit 1--Unlogged Corrected Error

This bit, when set, indicates a corrected error (or errors) occurred that would normally result in an entry in the CEL. However, the error could not be logged because the CEL already contained a valid entry.

Bits 9 through 11--Port Code Bits 0 through 2

These encoded bits indicate the CM port associated with the corrected error.

Code	Port
0	CP-0
1	IOU-0
2	CP-1
3	IOU-1

Bits 12 through 43--CM Address Bits 1 through 28, Parity Bits 0 through 3

These bits indicate the CM address associated with the corrected error.

Bits 48 through 55--Syndrome Code Bits 0 through 7

These bits indicate the CM syndrome code associated with the corrected error. Table B-9 describes each code.

Table B-9. SECDED Syndrome Codes/Corrected Bits

Code	Bit	Code	Bit	Code	Bit	Code	Bit
00	1	10	67 ²	20	66 ²	30	2/3 ³
01	71 ²	11	4	21	4	31	6
02	70 ²	12	4	22	4	32	6
03	6/7 ³	13	6	23	6	33	4
04	69 ²	14	4	24	4	34	6
05	4	15	6	25	6	35	4
06	4	16	6	26	6	36	4
07	24 ⁵	17	3	27	3	37	28 ⁵
08	68 ²	18	4	28	4	38	6
09	4	19	6	29	6	39	4
0A	4	1A	6	2A	6	3A	4
0B	16 ⁵	1B	3	2B	3	3B	20 ⁵
0C	4/5 ³	1C	6	2C	6	3C	4
0D	8 ⁵	1D	3	2D	3	3D	12 ⁵
0E	0 ⁵	1E	3	2E	3	3E	4 ⁵
0F	4	1F	6	2F	6	3F	4

Notes:

1. No error detected.
2. Syndrome code bit failed (single code bit set).
3. Double error or multiple error or forced double error due to a partial write parity error on one of the two bytes indicated.
4. Double error or multiple error (even number of code bits set).
5. Corrected single-bit error.
6. Multiple error reported as a single error.

(Continued)

Table B-9. SECDED Syndrome Codes/Corrected Bits *(Continued)*

Code	Bit	Code	Bit	Code	Bit	Code	Bit
40	65 ¹	50	2	60	2	70	56 ⁵
41	2	51	3	61	3	71	4
42	2	52	3	62	3	72	4
43	3	53	2	63	2	73	60 ⁵
44	2	54	3	64	3	74	4
45	3	55	2	65	2	75	58 ⁵
46	3	56	2	66	2	76	62 ⁵
47	4	57	26 ⁵	67	30 ⁵	77	4
48	2	58	3	68	3	78	4
49	3	59	2	69	2	79	57 ⁵
4A	3	5A	2	6A	2	7A	61 ⁵
4B	4	5B	18 ⁵	6B	22 ⁵	7B	4
4C	3	5C	2	6C	2	7C	59 ⁵
4D	4	5D	10 ⁵	6D	14 ⁵	7D	4
4E	4	5E	2 ⁵	6E	6 ⁵	7E	4
4F	3	5F	2	6F	2	7F	63 ⁵

Notes:

1. Syndrome code bit failed (single code bit set).
2. Double error or multiple error (even number of code bits set).
3. Multiple error reported as a single error.
4. Double error or multiple error.
5. Corrected single-bit error.

(Continued)

Table B-9. SECDED Syndrome Codes/Corrected Bits *(Continued)*

Code	Bit	Code	Bit	Code	Bit	Code	Bit
80	64 ¹	90	2	A0	2	B0	48 ⁵
81	2	91	3	A1	3	B1	4
82	2	92	3	A2	3	B2	4
83	3	93	2	A3	2	B3	52 ⁵
84	2	94	3	A4	3	B4	4
85	3	95	2	A5	2	B5	50 ⁵
86	3	96	2	A6	2	B6	54 ⁵
87	4	97	25 ⁵	A7	29 ⁵	B7	4
88	2	98	3	A8	3	B8	49 ⁴
89	3	99	2	A9	2	B9	49 ⁵
8A	3	9A	2	AA	2	BA	53 ⁵
8B	4	9B	17 ⁵	AB	21 ⁵	BB	21/53 ³
8C	3	9C	2	AC	2	BC	51 ⁵
8D	4	9D	9 ⁵	AD	13 ⁵	BD	4
8E	4	9E	1 ⁵	AE	5 ⁵	BE	4
8F	3	9F	2	AF	2	BF	55 ⁵

Notes:

1. Syndrome code bit failed (single code bit set).
2. Double error or multiple error (even number of code bits set).
3. Multiple error reported as a single error.
4. Double error or multiple error.
5. Corrected single-bit error.

(Continued)

Table B-9. SECDED Syndrome Codes/Corrected Bits *(Continued)*

Code	Bit	Code	Bit	Code	Bit	Code	Bit
C0	0/1 ¹	D0	40 ⁴	E0	32 ⁴	F0	5
C1	2	D1	40 ²	E1	32 ²	F1	3
C2	2	D2	44 ²	E2	36 ²	F2	3
C3	3	D3	44 ⁴	E3	36 ⁴	F3	5
C4	2	D4	42 ²	E4	34 ²	F4	3
C5	3	D5	42 ⁴	E5	34 ⁴	F5	5
C6	3	D6	46 ⁴	E6	38 ⁴	F6	5
C7	27 ⁴	D7	27/46 ²	E7	31/38 ²	F7	5
C8	3	D8	41 ²	E8	33 ²	F8	3
C9	5	D9	41 ⁴	E9	33 ⁴	F9	5
CA	5	DA	45 ⁴	EA	37 ⁴	FA	5
CB	19 ⁴	DB	19/45 ²	EB	23/37 ²	FB	23 ⁴
CC	5	DC	43 ⁴	EC	35 ⁴	FC	5
CD	11 ⁴	DD	11/43 ²	ED	15/35 ²	FD	15 ⁴
CE	3 ⁴	DE	3/47 ²	EE	7/39 ²	FE	7 ⁴
CF	5	DF	47 ⁴	EF	39 ⁴	FF	5

Notes:

1. Double error or multiple error or forced double error due to a partial write parity error on one of the two bytes.
2. Double error or multiple error.
3. Multiple error reported as a single error.
4. Corrected single-bit error.
5. Double error or multiple error (even number of code bits set).

Uncorrectable Error Log 1 (UEL1/A4)

CMC contains a 64-bit UEL1 that contains the following information about an uncorrectable error.

Bit 0--Valid Bit

This bit, when set, indicates the presence of a valid entry in the log.

Bit 1--Unlogged Uncorrected Error

This bit, when set, indicates an uncorrectable error (or errors) occurred that would normally result in an entry in the UEL1. However, the error could not be logged because the UEL1 already contained a valid entry.

Bit 2--Multiple-Bit Error

This bit, when set, indicates two or more SECDED errors occurred in CM.

Bits 3 through 7--Function Code Bits 0 through 3, Parity

These encoded bits indicate the CM function being performed when the corrected error occurred. All other codes are illegal.

Code	Function
0	Read
2	Write
4	Read and Set Lock
5	Read and Clear Lock
6	Exchange
A	Read Free Running Counter
B	Refresh Counter Resync
C	Interrupt

Bit 8--Mark Parity Bit

This is the parity bit for bits 56 through 63 (mark bits 0 through 7).

Bits 9 through 11--Port Code Bits 0 through 2

These encoded bits indicate the CM port associated with the uncorrectable error.

Code	Port
0	CP-0
1	IOU-0
2	CP-1
3	IOU-1

Bits 12 through 43--CM Address Bits 1 through 28, Parity Bits 0 through 3

These bits indicate the CM address associated with the uncorrectable error.

Bits 44 through 47--Parity Error Code Bits 0 through 3

These encoded bits indicate the type of parity error that occurred.

Bits**44-47 Description**

1111	CM address byte 3 parity error II
1110	CM address byte 2 parity error II
1101	CM address byte 1 parity error II
1100	CM address byte 0 parity error II
1011	CM address byte 3 parity error I
1010	CM address byte 2 parity error I
1001	CM address byte 1 parity error I
1000	CM address byte 0 parity error I
0111	CM address byte 3 parity error
0110	CM address byte 2 parity error
0101	CM address byte 1 parity error
0100	CM address byte 0 parity error
0011	Tag parity error
0010	Mark parity error
0001	Function code parity error
0000	No error

Bits 48 through 55--Write Parity Error Bytes 0 through 7

These bits, when set, indicate which byte(s) had a parity error during a CM write operation.

Bits 56 through 63--Mark Bits 0 through 7, Parity

These bits, when set, indicate the corresponding byte was written to CM when the uncorrectable error occurred.

Uncorrectable Error Log 2 (UEL2/A8)

CMC contains a 64-bit UEL2 that contains the following information about an uncorrectable error. Bits 5 through 8 and 44 through 47 are not used.

Bit 0--Valid Bit

This bit, when set, indicates the presence of a valid entry in the log.

Bit 1--Unlogged Uncorrectable Error

This bit, when set, indicates an uncorrectable error (or errors) occurred that would normally result in an entry in the UEL2. However, the error could not be logged because the UEL2 already contained a valid entry.

Bit 2--Illegal Function

This bit, when set, indicates an illegal function (1, 3, 7, D through F) was attempted.

Bit 3--Bounds Fault

This bit, when set, indicates an address was outside established boundaries in CM.

Bit 4--Write Data Byte 7 Parity Error

This bit, when set, indicates that byte 7 had a parity error during a CM write operation.

Bits 9 through 11--Port Code Bits 0 through 2

These encoded bits indicate the CM port associated with the uncorrectable error.

Code	Port
0	CP-0
1	IOU-0
2	CP-1
3	IOU-1

Bits 12 through 43--CM Address Bits 1 through 28, Parity Bits 0 through 3

These bits indicate the CM address associated with the uncorrectable error.

Bits 48 through 55--Read Data Parity Error Bytes 0 through 7

These bits, when set, indicate which byte(s) had a parity error during a CM read operation.

Bits 56 through 63--Partial Write Data Parity Error Bytes 0 through 7

These bits, when set, indicate which byte(s) had a parity error during a CM partial write operation.

Maintenance Register Worksheet

Figure B-9 is a worksheet for recording maintenance register contents.

	0000	0000	0011	1111	1111	2222	2222	2233	3333	3333	4444	4444	4455	5555	5555	6666
	0123	4567	8901	2345	6789	0123	4567	8901	2345	6789	0123	4567	8901	2345	6789	0123
	CPU															
(SS) 00																
(EID) 10																
(OI) 12																
(DEC) 30																
(PFS) 80																
(PFS) 81																
(PFS) 82																
(PFS) 83																
(PFS) 84																
(PFS) 85																
(PFS) 86																
(PFS) 87																
(PFS) 88																
(PFS) 89																
(PTM) A0																
	CM															
(SS) 00																
(EID) 10																
(OI) 12																
(EC) 20																
(CEL) A0																
(UEL1) A4																
(UEL2) A8																
	IOU															
(SS) 00																
(EID) 10																
(OI) 12																
(FSM) 18																
(OSB) 21																
(EC) 30																
(SR) 40																
(FS1) 80																
(FS2) 81																
(TM) A0																
	0000	0000	0011	1111	1111	2222	2222	2233	3333	3333	4444	4444	4455	5555	5555	6666
	0123	4567	8901	2345	6789	0123	4567	8901	2345	6789	0123	4567	8901	2345	6789	0123

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Figure B-9. Maintenance Register Worksheet

Deadstart Display Features (960 Only) C

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Deadstart Display Features (960 Only)

C

The deadstart display features described in this appendix allow for deadstarting the system and performing basic maintenance functions in the IOU. These include commands that may be entered at the system console keyboard by the user and the displays associated with those commands. The deadstart display features are supported via the program memory of the two-port multiplexer (TPM) microprocessor contained in the IOU; it is not necessary for a program to be operational in the PPs.

The capabilities of the deadstart display features arise out of the ability of the TPM to share the maintenance access control (MAC) circuits with channel 17. The TPM obtains control of these circuits when the deadstart display is activated, and does not release control until the deadstart display is released. The completion of a deadstart sequence or the execution of an RT command releases the deadstart display.

Hardware Interface

NOTE

System consoles are supported only when they are running Viking X emulation software and only by TPM firmware revisions 12 and later.

The hardware interface for a system console is, in most respects, identical to the interface for a Viking X compatible display console. There are only two differences.

1. On IOU 0, the system console is connected directly to both TPM ports. On IOU 1, a system console may only be connected to TPM port 0.
2. Remote users may gain access to the TPM by dialing up the system console, which is responsible for answering the phone and routing the remote user's commands to port 1. Refer to the 19003 System Console Hardware Operations/Maintenance manual for information concerning the displays presented and the options available to a user dialing into a system console.

The second difference is in the format and speed of the data transferred between the console and the TPM. It is possible for the system console and the TPM to exchange data at a baud rate of 38.4K; this option is not available with Viking X compatible consoles. In addition, the system console normally communicates using an 8 data bit, 1 stop bit format; the Viking X normally uses a 7 data bit, 2 stop bit format.

NOTE

It is possible to use the Deadstart Display on either port to inspect internal data on a running system with the following restrictions:

- Any PP attempting to use channel 17 (the maintenance access channel) while the Deadstart Display is active will hang.
 - The software currently running in the PPs must not attempt to use channel 15 TPM or calendar clock features.
 - The following displays and commands are potentially destructive:
 - PP Memory Display (PM)
 - Enter PP Memory Commands (EP, EP+, EM)
 - Enter Maintenance Register Command (ER, ER+)
 - Any of the commands to reconfigure, idle, or deadstart.
 - Power-on reset (*R)
 - Move PP Memory Command (MP)
 - Master Clear and Clear Errors (MC)
 - Extend PP Memory (XM)
 - IOU Initialization (I)
 - Internal Diagnostic Tests (D, DT)
-

Software Interface

NOTE

System consoles are supported only when they are running Viking X emulation software and only by TPM firmware revisions 12 and later.

The system console Console Main Menu is activated after the user types **Ctrl-G** (e.g., presses the **G** key while holding down the **Ctrl** key) or **Ctrl-F2** at the console keyboard. Pressing these keys cause the system console to clear the screen and paint the Console Main Menu (figure C-1), but has no effect on the TPM microprocessor, channel 15 or channel 17. Once this display is on the screen, the user may choose one of several options. Among the choices available on the Console Main Menu are:

- Selecting System Load Options
- Selecting Console Utilities
- Advancing to the Maintenance Options Display

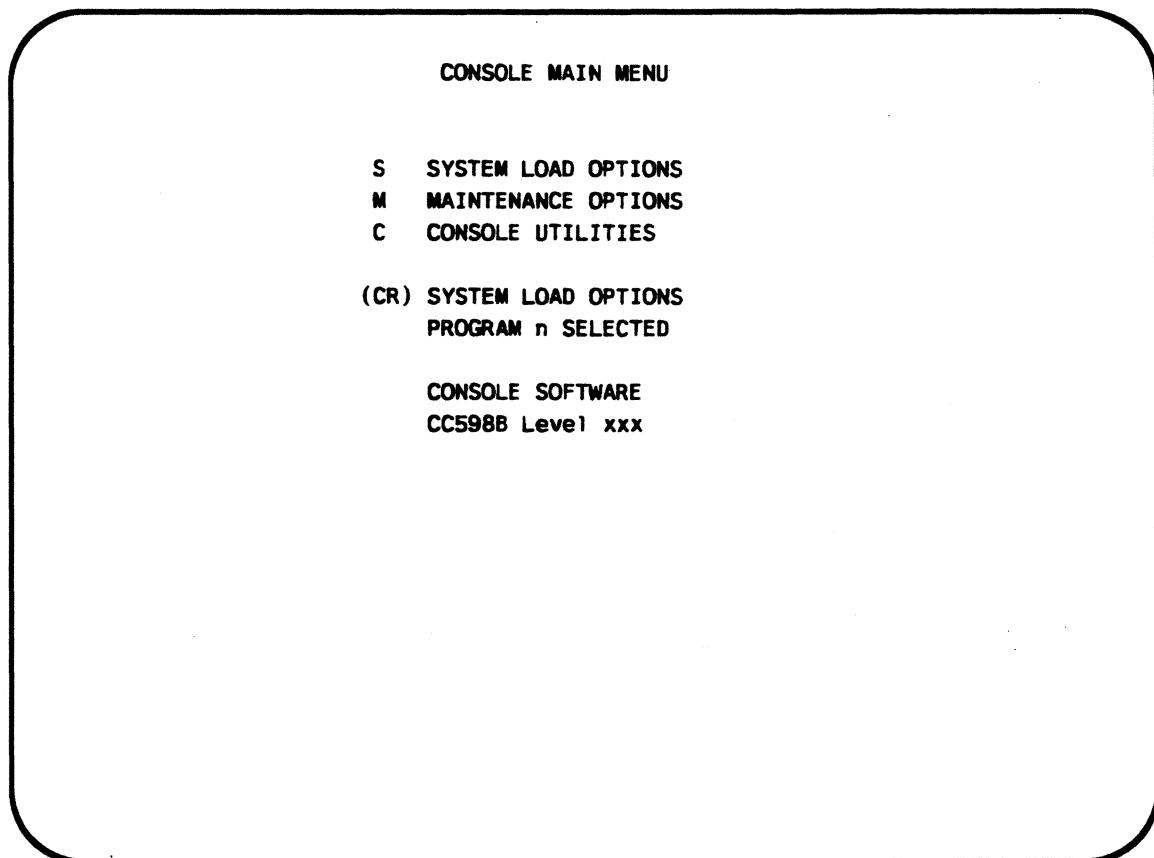


Figure C-1. Console Main Menu

To present the information in this chapter in a structured format, this page has been left blank.

When M (Maintenance Options) is selected from the Console Main Menu on a single-IOU system, the IOU 0 Maintenance Options Display shown in figure C-2 appears. When M is selected from the Console Main Menu on a dual-IOU system, an intermediate display appears that allows the user to advance to the IOU-0 Maintenance Options Display by typing 0, or to advance to an IOU-1 Maintenance Options Display by typing a 1. A selection is also available to perform a system load with a long deadstart by typing L.

MAINTENANCE OPTIONS - IOU 0	
MODEL 40 (S/N 0303) REV. 15	
XX YYYYYY-CHANGE DS PRG	PROGRAM 0
XX+YYYYYY-CHANGE DS PRG INC	01 001402
S-SHORT DS	02 007302
L-LONG DS	03 000017
H-HELP	04 007502
	05 007702
	06 000341
	07 007402
PPM CONF = 0	10 007102
NIO BRL CONF = 0	11 007301
DLY LOOP = 0	12 000730
LDS ADDR = 6000	13 000000
CLK FREQ = NORMAL	14 000000
NIO MEM SIZE = 8K	15 000000
STAT SUM = 10	16 000000
	17 000000
	20 007112

Figure C-2. IOU 0 Maintenance Options Display

Headstarting the PPs

There are two basic commands provided to deadstart the PPs: S and L. Command S is used to initiate a short deadstart sequence. Command L is used to initiate a long deadstart sequence. These commands are described in the following paragraphs.

Command S

Command S (followed pressing **Enter**) is used to initiate a short deadstart sequence. In this sequence, a deadstart master clear is issued to the PPs and I/O channels and the program currently displayed on the screen is loaded into logical PP0. Execution begins at word 1 of this program. At the end of the sequence, the screen of the system console is blanked in preparation for use by the software being deadstarted in PP0. (Note that the program used is the one displayed on the screen and does not necessarily have to be the same as one of the permanently stored special purpose programs.)

Command L

Command L (followed by pressing **Enter**) is used to initiate a long deadstart sequence. In this sequence, the following events occur:

- A deadstart master clear is issued to the PPs and channels, and all error status bits are cleared.
- The long deadstart program, permanently stored in the TPM program memory, is loaded into logical PP0 and executed. This program performs a diagnostic test that checks out the major hardware elements required for deadstart.
- The PP register display is brought up on the right-hand side of the screen while the long deadstart program is running. (This program runs for about 15 seconds.)
- Certain error status bits are monitored to determine if the hardware failed during the long deadstart. In case of failure, one of the following messages is displayed below the PP register display. Refer to figure C-3.)

BRANCH TEST FAILURE

This error message appears when the branch test portion of the long deadstart diagnostic fails.

TFR ERR XXXXX YYYYYY (ZZZZZ) Program Transfer Error

This error message appears when the TPM is unable to load the long deadstart diagnostic into PP0, where

XXXXXX = The failing PP0 address

YYYYYY = The data the TPM attempted to load into PP0

ZZZZZ = The data the TPM read back from address XXXXX after loading that address with YYYYYY

STATUS SUMMARY ERROR

For IOU errors only. The TPM clears all fault status register errors before beginning the long deadstart diagnostic. However, this message will appear during the diagnostic execution if the diagnostic causes an error. Refer to the Maintenance Register Display for error isolation information.

- If the program runs to completion without error, then a short deadstart sequence is automatically initiated, using the program currently displayed on the screen.

MAINTENANCE OPTIONS - IOU 0				
MODEL 40 (S/N XXXX) REV. 15				
XX YYYYYY-CHANGE DS PRG	PROGRAM 0	+ADU BUSY	NIO BARREL=0	
XX+YYYYYY-CHANGE DS PRG INC	01 000300	*=PP IDLE	EX BUSY=0	
S-SHORT DS	02 000000			
L-LONG DS	03 000000	PP P A Q K		
H-HELP	04 000000	*+00 000001 007757 000001 107700		
	05 000000	+01 007777 010000 000001 007100		
	06 000000	* 02 007777 010000 000002 107700		
	07 000000	03 007777 010000 000003 007100		
	10 000000	04 007777 010000 000004 007100		
PPM CONF = 0	11 000000			
NIO BRL CONF = 0	12 000000			
DLY LOOP = 0	13 000000			
LDS ADDR = 6000	14 000000			
CLK FREQ = NORMAL	15 000000			
NIO MEM SIZE = 4K	16 000000	BRANCH TEST FAILURE		
STAT SUM = 14	17 000000	TFR ERR XXXXX YYYYYY (ZZZZZZ)		
	20 000000	STATUS SUMMARY ERROR		
ERROR MESSAGES		BATTERY FAILURE		
KEYBOARD ECHO		RE-ENTER DS PROGRAMS		

Figure C-3. PP Register Display Showing LDS Errors

Deadstart Programs

The short deadstart sequence causes the 16-word program currently displayed on the console to be loaded into locations 1 through 208 of PP0, and causes execution of the program to begin at location 1. Commands are provided to enter or modify this program. Multiple programs may be created for different uses and may be saved in a special memory. Four such programs may be stored using the command:

SP X Store Program (0 through 3)

where X is the program number (X = 0 through 3). Once a program has been stored, it may be retrieved and displayed at a later time by using the command:

GP X Get Program (0 through 7)

where X is the program number to be retrieved and displayed.

In addition to the four programs that may be stored using the SP command, there are four more (fixed) programs that can be accessed using the GP command. These programs are numbered 4 through 7. Hence, allowable values of the parameter X are 0 through 7. (Programs 4 through 7 are intended for maintenance use.) After a GP command, the program number X is displayed on the screen for reference only. If any editing of the program is done, only the local or "screen" version is changed. The original version in location X is not modified because stored programs can only be changed by an SP X command. (Note that it is possible to get a program from one location, perform editing, and save it in a different location, if desired.)

The user may inspect each of the deadstart programs, one after the other, by pressing the **space bar**. If the only entry in a command line is via the **space bar**, the next higher numbered deadstart program is displayed. After program 7 is selected, program 0 is re-selected.

Permanent Deadstart Programs 4 Through 7

Four special purpose programs are permanently stored in the TPM memory for use by maintenance personnel. These programs should not be executed by the operator unless the customer engineer requests them.

The programs may be retrieved and displayed by using the GP X (Get Program X) command, where X is the program number. The contents of the programs are shown in figures C-4 through C-6. The maintenance functions performed by the programs are as follows:

Program 4: Chain Test, Lower Channels - This program tests the internal channel registers by passing a simple program from one PP to the next. The transfer takes place on the channel that has the same number as the logical PP which is to receive the program. Hence, channels 1 through 11 are tested.

The program begins execution in PP0 and completes when the last PP in the chain hangs while trying to pass the program to the next (non-existent) PP. At completion time PP 11 attempts to output on channel 12.

Program 5: Chain Test, Upper Channels - This program is similar to program 4, except that PPs 20 through 31 are used to test channels 20 through 31.

Program 6: Clear Errors and Clear ADU - This utility issues the master clear and clear errors functions to the IOU, memory, and the CPU.

Program 7: Not used.

STORED DEADSTART PROGRAM 4			
Mnemonic		Location	Code
AOD	5B	01	003605
AOD	7B	02	003607
AOD	11B	03	003611
LDN	00B	04	001400
OAN	00B	05	007200
LDN	20B	06	001420
OAM	1B	07	007300
		10	000001
DCN	00B	11	007500
LCN	00B	12	001500
SHN	-2B	13	001075
LMDL	20B	14	103320
NJN	*	15	000500
UJN	*	16	000300
DATA	0	17	000000
DATA	17777B	20	177777

Figure C-4. Stored Deadstart Program 4 - Chain Test, Lower Channels

STORED DEADSTART PROGRAM 5

Mnemonic		Location	Code
AOD	5B	01	003605
AOD	7B	02	003607
AOD	11B	03	003611
LDN	00B	04	001400
OAN	17B	05	007217
LDN	20B	06	001420
OAM	1, 17B	07	007317
		10	000001
DCN	17B	11	007517
LCN	00B	12	001500
SHN	-2B	13	001075
LMDL	20B	14	103320
NJN	*	15	000500
UJN	*	16	000300
DATA	0	17	000000
DATA	177777B	20	177777

Figure C-5. Stored Deadstart Program 5 - Chain Test, Upper Channels

STORED DEADSTART PROGRAM 6			
Mnemonic		Location	Code
DCN	17B	01	007517
FNC	540B, 17B	02	007717
		03	000540
FNC	140B, 17B	04	007717
		05	000140
FNC	552B, 17B	06	007717
		07	000552
FNC	560B, 17B	10	007717
		11	000560
FNC	572B, 17B	12	007717
		13	000572
FNC	160B, 17B	14	007717
		15	000160
UJN	*	16	000300
		17	000000
		20	000000

Figure C-6. Stored Deadstart Program 6 - Clear Errors and Clear ADU

Editing Deadstart Programs

Two commands are provided to edit a program displayed on the screen, these are:

```
XX YYYYYY (or XX.YYYYYY or XX,YYYYYY)
and
XX+YYYYYY
```

The first command is used to change a single word (XX) in the program to a new value (YYYYYY). The number YYYYYY may be any number having from one to six octal digits and in the range 0 through 177777. Leading zeros do not have to be typed for XX or YYYYYY.

The second command is used to change a block of sequential words in the program. As each new word is entered, the editor automatically increments the address value XX and clears the remainder of the line so that the value at the (incremented) address may be entered. Pressing the **Enter** key before entering a data value will cause the old value to remain unaffected and will increment to the next XX. This block editing may be terminated by pressing the **Esc** key. Alternatively, the sequence is terminated automatically when word number 20 has been entered.

Reconfiguration

In order to deadstart NOS or NOS/VE, it is necessary that logical PPs 0, 1, 2, and 10 (octal) be functional. If they are functional, then the system may be deadstarted and other (failing) PPs may be logically turned off using the CTI commands described under the Operator Intervention Display in the Disk Deadstart section of the CIP Reference manual. If, however, one of these PPs is not functional, then hardware reconfiguration should be used as described below to select a set of logical PPs from the available physical PPs such that logical PPs 0, 1, 2, and 10 in the barrel are good.

Hardware reconfiguration of PPs is accomplished by a combination of reconfiguring barrels and PP memories. NIO barrels are reconfigured by using the deadstart display and typing the command:

```
RB X
```

where X is the number of the NIO barrel which is to be used as logical barrel 0 and which will contain logical PP0. That is, physical NIO barrel X will become logical barrel 0. The value X, which may be 0, 1, 2 or 3, is displayed on the line NIO BRL CONF=X of the Maintenance Options Display. Note that CIO barrels are not affected by the RB command.

PP memories within each barrel may be reconfigured by using the deadstart display and typing the command:

```
RP X
```

where X is the number of the physical PP memory that is to be used as logical PP memory 0. Note that X not only designates which PP in logical barrel 0 is to be PP0; it also designates which PP in logical barrel 1 will be PP5, which PP in barrel 2 will be PP20, and which PP in barrel 3 will be PP25. The value X, which may be 0, 1, 2, 3 or 4, is displayed on the line PPM CONF=X of the Maintenance Options Display.

For examples of the effects of reconfiguration, refer to figures C-7 and C-8.

NOTE

The RB command takes effect as soon as it is entered. The RP command takes effect only after a master clear has been issued, even though the PPM CONF=X line is updated when the command is entered. Commands that cause a deadstart master clear are S, L, DS, and SD. Certain packets also cause a master clear to be issued.

PHYSICAL PPMs IN EACH BARREL	NIO LOGICAL PP NUMBERS															
	RB=0				RB=1				RB=2				RB=3			
	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3
00	00	05	20	25	25	00	05	20	20	25	00	05	05	20	25	00
01	01	06	21	26	26	01	06	21	21	26	01	06	06	21	26	01
02	02	07	22	27	27	02	07	22	22	27	02	07	07	22	27	02
03	03	10	23	30	30	03	10	23	23	30	03	10	10	23	30	03
04	04	11	24	31	31	04	11	24	24	31	04	11	11	24	31	04

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PHYSICAL PPMs IN EACH BARREL	CIO LOGICAL PP NO.	
	BAR0	BAR1
00	00	05
01	01	06
02	02	07
03	03	10
04	04	11

NOTES:

RB = NIO BARREL CONFIGURATION (NOT APPLICABLE TO CIO BARRELS).

BAR0-3 ARE THE PHYSICAL BARRELS.

Figure C-7. Reconfiguration Example, RP = 0

PHYSICAL PPMs IN EACH BARREL	NIO LOGICAL PP NUMBERS															
	RB=0				RB=1				RB=2				RB=3			
	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3
00	03	10	23	30	30	03	10	23	23	30	03	10	10	23	30	03
01	04	11	24	31	31	04	11	24	24	31	04	11	11	24	31	04
02	00	05	20	25	25	00	05	20	20	25	00	05	05	20	25	00
03	01	06	21	26	26	01	06	21	21	26	01	06	06	21	26	01
04	02	07	22	27	27	02	07	22	22	27	02	07	07	22	27	02

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PHYSICAL PPMs IN EACH BARREL	CIO LOGICAL PP NO.	
	BAR0	BAR1
00	03	10
01	04	11
02	00	05
03	01	06
04	02	07

NOTES:

RB = NIO BARREL CONFIGURATION (NOT APPLICABLE TO CIO BARRELS).

BAR0-3 ARE THE PHYSICAL BARRELS.

Figure C-8. Reconfiguration Example, RP = 2

Maintenance Features

The following paragraphs describe the deadstart maintenance commands and displays. These commands and displays may be used for troubleshooting hardware failures or for diagnosing problems with system software. They allow inspection of the internal PP data and control information. In addition, they provide a means of establishing hardware scope loops for looking at failing hardware conditions.

To execute these commands, the user must first reach the Maintenance Options Display (figure C-2). Refer to the Software Interface description for instructions on selecting the Maintenance Options Display. The R command will return to the Maintenance Options Display from any of the other maintenance displays described in this appendix.

The following commands are intended to be used by the customer engineer only and should not be executed by the operator.

- TB XX YYYYYY
- DE X
- LA YYYY
- SM
- SD
- DS

CF X (Clock Frequency)

This command is used to select the 20-MHz clock frequency margin condition. Parameter X may be F (2% faster), N (normal), or S (2% slower). It is initialized to normal when the system is powered up or the 1JKH module is inserted. Note that the clock frequency display may be erroneous if modules have been removed and reinserted with power on. A new clock frequency takes effect when a deadstart is performed. The commands that perform a deadstart are S, L, and DS.

CH W (Channel Status Display)

This command causes channel status information to be displayed as shown in figures C-9 and C-10. The W parameter may either be N to select the NIO channels or C to select the CIO channels. Possible values for the signals displayed are 0 and 1. Note that NIO channel 16 is not implemented.

IOU 0 CIO CHANNEL STATUS											
	00	01	02	03	04	05	06	07	10	11	
ACTIVE	0	0	1	1	1	1	1	1	1	1	
FULL	0	0	0	0	0	0	0	0	0	1	
FLAG	0	0	0	0	0	0	0	0	0	0	
ERROR	0	0	0	0	0	0	0	0	0	0	

ERROR MESSAGES	RE-ENTER DS PROGRAMS
KEYBOARD ECHO	

Figure C-9. Channel Status Display, CIO Channels

IOU 0 NIO CHANNEL STATUS

	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17
DIS PE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
ACTIVE	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
FULL	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0
FLAG	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
ERROR	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

	20	21	22	23	24	25	26	27	30	31	32	33
DIS PE	0	0	0	0	0	0	0	1	0	0	0	0
ACTIVE	0	0	0	0	0	0	0	0	0	0	0	0
FULL	0	0	0	0	0	0	0	0	0	0	0	0
FLAG	0	0	0	0	0	0	0	0	0	0	0	0
ERROR	0	0	0	0	0	0	0	0	0	0	0	0

ERROR MESSAGES

RE-ENTER DS PROGRAMS

KEYBOARD ECHO

Figure C-10. Channel Status Display, NIO Channels

CL (Clear LEDS)

This command is used to clear the fault LEDs on all IOU modules.

DC WXX (Deadstart Channel)

This command deadstarts just the specified channel. The parameter WXX must be an octal number in either the range N0 through N13, N20 through N33, or C0 through C11. The parameter N designates an NIO channel, and C designates a CIO channel.

DE X (Delay)

This command selects one of eight loop delay times for use with those commands which perform repeated deadstarts (SD, S and L). The parameter X may have values 0 through 7, and is used to select the delay time from a fixed table. The times in the table are arranged from shortest (X = 0) to longest (X = 7) in logarithmic steps. Deadstart programs that execute quickly may use short delay times for maximum brightness of the oscilloscope trace. Alternatively, the delay time may be increased for longer programs to allow for full execution when scoping, or to allow time for the program to complete before the register display is updated when using the SD feature. New delay values may be entered at any time.

Loop time ranges:

S - 1.7 ms to 10.33 ms

L - 244 us to 8.85 ms

SD - 205 ms to 346 ms (Besides the DE value, SD times also depend on which display is currently being viewed.)

DS (Deadstart and Return-To-Deadstart Display)

This command causes a deadstart master clear to be issued and the 208 word deadstart program displayed on the screen to be loaded into PP 0 and executed. After allowing the program to execute for about 340 microseconds, the TPM microprocessor reverts to its deadstart display mode and reactivates the display that was present on the screen before the DS command was entered.

EM XXXXX YYYYY ZZZZZZ (Enter PP Memory Block)

The EM command is used to enter data pattern ZZZZZZ into the PP memory currently displayed starting from location XXXXX through location YYYYY. The parameters are similar to those of the EP command. This command may be used only when the PP memory display is active.

EP XXXXX YYYYYY (Enter PP Memory)

This command may be used when the PP memory display is active to enter data YYYYYY into location XXXXX of the PP memory currently displayed on the screen. The command may also be used in the format:

EP+XXXXX YYYYYY

This format automatically increments the address XXXXX after each entry to facilitate entering sequential blocks of data. The use of the Return key and no new data will merely increment to the next PP memory address. Sequential data entry using this second format is terminated by pressing the Erase key. The parameter XXXXX may be any octal number in the range 0 through 17777 (0 through 7777 for NIO in normal mode), and the parameter YYYYYY may be any octal number in the range 0 through 177777. These commands may be used to perform octal patches on test programs, or to enter troubleshooting routines which are longer than 16 words and therefore, do not fit in a normal deadstart program. In the latter case, the program entered using this command should be placed beyond word 21 (because the deadstart sequence over-writes words 0 through 21) and the deadstart program should contain a jump to the beginning of the test program.

ER XX Y ZZ (Enter Register)

This command may be used to modify contents of the PP maintenance registers whenever the Maintenance Register Display is active. The parameters are as follows:

XX = Register number (as described under command MR - Maintenance Register Display)

Y = Byte number (0 through 7)

ZZ = Hexadecimal data to be entered (0 through FF).

FI WXX (Force Idle)

This command forces a PP idle. The parameter WXX, the number of the logical PP to be idled, may be any octal number in either the range of N0 through N11, N20 through N31, or C0 through C11. All idled PPs are reactivated by a short (S) or a long deadstart (L).

The FI WXX command may be useful in debugging software that ties up a system element (such as memory, a channel, etc.) In such a case, the Maintenance Options Display should be activated, the failing PP idled, and the PP registers inspected. Note that activating the Maintenance Options Display on a TPM port terminal, both ports, as well as channel 17, become unavailable. Either case could result in a PP hang, so this procedure should only be used during time dedicated to software testing.

H (Help Display)

Figures C-11 and C-12 show the contents of the two Help displays that are available to the user. These figures list the various commands and their definitions that can be input from the keyboard to change deadstart programs or invoke maintenance displays. For example: Type H followed by **Enter** to view Help Display, Page 0 on the console screen. Type + (**Enter**) to toggle to Help Display, Page 1. Type R (**Enter**) to return to the Maintenance Options Display.

HELP DISPLAY	
R	RETURN TO MAINT OPTIONS DISPLAY
I	INITIALIZE IOU
GP X	GET DS PRO 0-7
	RAM USER PRG 0-3
	EPROM MAINT PRG 4-7
SPACE BAR	SELECT NEXT DS PRG
SP X	STORE TO DS PRG 0-3
TB XX YYYYYY	TOGGLE BITS YYYYYY IN DS WORD XX
SD	SHORT DS DISPLAY LOOP
DE X	SET LOOP DELAY 0-7
SM	ARM SCOPE MODE
CH W	PP CHAN STATUS DISPLAY N/C
PS XX YYY	NIO CH XX PARITY SWITCH ON/OFF
DC WXX	DS CH N0-13,N20-33,C0-11
CL	CLEAR LEDS
DS	ISSUE SDS/MC AND KEEP DISPLAY
MC	CLEAR ADU AND CLEAR ERRORS
CF X	SET CLOCK FREQ F,N OR S
ERROR MESSAGES	
(TYPE + TO TOGGLE)	
KEYBOARD ECHO	

Figure C-11. Help Display, Page 0

HELP DISPLAY

RP X	SET PP MEM CONFIG 0-4
RB X	SET NIO BRL CONFIG 0-3
LA YYYY	SET LDS START ADDR
XM XXX	EXTEND NIO MEM SIZE ON/OFF(8K/4K)
PM WXX YYYY	DISPLAY PPM N/C XX STARTING YYYY
+	INC PPM ADDR
-	DEC PPM ADDR
EP XXXXX YYYYYY	ENTER DATA YYYYYY IN PPM LOC XXXXX
EP+XXXXX YYYYYY	AS ABOVE BUT INC ADDR
EM XXXXX YYYYY ZZZZZ	PPM PATTERN ZZZZZZ AT XXXXX TO YYYYY
MP WXX YY	MOVE PPM FROM PP N/C XX TO PP N/C YY
PR WX	PP REG DISPLAY N/C BRL X
+(-)	INC(DEC) LOGICAL BRL FOR REG DISPLAY
FI WXX	IDLE PP N/C XX
MR	PP MAINT REG DISPLAY
+	TOGGLE MAINT REG DISPLAY
ER XX Y ZZ	ENTER HEX DATA ZZ BYTE Y, MAINT REG XX
ER+XX Y ZZ	AS ABOVE BUT INC BYTE

ERROR MESSAGES

(TYPE + TO TOGGLE)

KEYBOARD ECHO

Figure C-12. Help Display, Page 1

I (IOU Initialization)

This command returns the IOU to its power-up state. It causes the TPM microprocessor to perform the following operations in the order shown:

1. Disarm scope mode.
2. Set the IOU clock frequency to normal.
3. Idle all PPs.
4. Clear all PP memories in 8K mode.
5. Master clear the assembly/disassembly unit (ADU).
6. Clear fault status register errors.
7. Clear the operating system bounds registers.
8. Clear the module LEDs.
9. Set all P, A, K and Q registers to their deadstart state.
10. Set all channels to their deadstart state.
11. Idle NIO PP 0.
12. Bring up the Deadstart Options Display.

The message IOU INITIALIZATION IN PROGRESS appears on the screen while the PP memories are being cleared.

LA YYYY (Long Deadstart Address)

This command and its usage is normally restricted to factory use only. The address at which a long deadstart (LDS) begins may be set to the value YYYY through use of this command. The parameter YYYY may be any octal number in the range 0 through 7776, with 6000 being the setting for a normal LDS. Values other than 6000 may be desirable when the first portion of the LDS program runs successfully, and the hardware problem being investigated causes a failure beyond the point where a scope loop would be short enough to be feasible. In these cases, the LA command may be used to set YYYY to an address just before the point of failure, resulting in a usable scope loop. Workable starting addresses may be determined using the LDS program listing.

Loop time may be adjusted using the DE command. Note the following:

- Whenever this command is used, care should be taken to always return YYYY to the normal value of 6000.
- The YYYY parameter is always reset to 6000 at IOU power-up time.
- Addresses less than 6000 are not part of the LDS program and are executed using the pre-deadstart contents of PP0 memory.
- LDS causes PP0 addresses of 6000 and above to be overwritten with the LDS program that is stored in the TPM read-only memory.

MC (Master Clear)

This command master clears the ADU and also clears IOU errors.

MP WXX WYY (Move PP Memory Into Another PP Memory)

This command is used to copy the entire 8K contents in PP memory WXX to PP memory WYY. If either of the PP memories is an NIO memory in normal (4K) mode, only the lower 4K is transferred.

MR (Maintenance Register Display)

This command causes the contents of the IOU maintenance registers to be displayed on the right-hand side of the screen (figures C-13 and C-14). The display consists of 8 or 16 lines, and each line consists of the register number (in hexadecimal) followed by 16 hexadecimal digits grouped in pairs (bytes) for ease of reading. (Refer to appendix B for definitions of the codes.) The first group of registers displayed are as follows (figure C-13):

Register	Number	Description
NIO	12	Options Installed Register
	18	Fault Status Mask Register
	21	Operating System Bounds Register
	30	Environment Control Register
	40	Status Register
	80	Fault Status 1 Register
	81	Fault Status 2 Register
	A0	Test Mode Register
CIO	16	Options Installed Register
	1C	Fault Status Mask Register
	25	Operating System Bounds Register
	34	Environment Control Register
	44	Status Register
	84	Fault Status 1 Register
	85	Fault Status 2 Register
	A4	Test Mode Register

MAINTENANCE OPTIONS - IOU 0
MODEL 40 (S/N XXXX) REV. XX

XX YYYYYY-CHANGE DS PRG	PROGRAM 0	NIO	IOU MAINT REG
XX+YYYYYY-CHANGE DS PRG INC	01 000300	12 00	00 00 00 00 00 01 00
S-SHORT DS	02 000000	18 00	00 03 FF AF 00 00 00
L-LONG DS	03 000000	21 00	00 00 00 00 00 00 00
H-HELP	04 000000	30 00	00 00 00 00 00 00 00
	05 000000	40 00	00 00 00 00 00 00 00
	06 000000	80 00	00 00 00 00 00 00 00
	07 000000	81 00	00 00 00 00 00 00 00
PPM CONF = 0	10 000000	A0 00	00 00 00 00 00 00 00
NIO BRL CONF = 0	11 000000	CIO	
DLY LOOP = 0	12 000000	16 00	00 00 00 00 00 00 00
LDS ADDR = 0	13 000000	1C 00	00 00 00 00 00 00 00
CLK FREQ = NORMAL	14 000000	25 00	00 00 00 00 00 00 00
NIO MEM SIZE = 4K	15 000000	34 00	00 00 00 00 00 00 00
STAT SUM = 00	16 000000	44 00	00 00 00 00 00 00 00
	17 000000	84 00	00 00 00 00 00 00 00
	20 000000	85 00	00 00 00 00 00 00 00
		A4 00	00 00 00 00 00 00 00
ERROR MESSAGES			BATTERY FAILURE
KEYBOARD ECHO			RE-ENTER DS PROGRAMS

Figure C-13. Maintenance Register Display, Page 0

Register Number	Description
B0	CIO Channel 0 Status Register
B1	CIO Channel 1 Status Register
B2	CIO Channel 2 Status Register
B3	CIO Channel 3 Status Register
B4	CIO Channel 4 Status Register
B5	CIO Channel 5 Status Register
B6	CIO Channel 6 Status Register
B7	CIO Channel 7 Status Register
B8	CIO Channel 10 Status Register
B9	CIO Channel 11 Status Register

	CIO	IOU MAINT REG
XX YYYYYY-CHANGE DS PRG	PROGRAM 0	
XX+YYYYYY-CHANGE DS PRG INC	01 000300	B0 00 00 00 03 22 00 01 00
S-SHORT DS	02 000000	B1 00 00 00 00 22 00 00 00
L-LONG DS	03 000000	B2 00 00 00 00 22 00 00 00
H-HELP	04 000000	B3 00 00 00 00 22 00 00 00
	05 000000	B4 00 00 00 00 22 00 00 00
	06 000000	B5 00 00 00 00 22 00 00 00
	07 000000	B6 00 00 00 00 22 00 00 00
PPM CONF = 0	10 000000	B7 00 00 00 00 22 00 00 00
NIO BRL CONF = 0	11 000000	B8 00 00 00 00 22 00 00 00
DLY LOOP = 0	12 000000	B9 00 00 00 00 22 00 00 00
LDS ADDR = 6000	13 000000	
CLK FREQ = NORMAL	14 000000	
NIO MEM SIZE = 4K	15 000000	
STAT SUM = 00	16 000000	
	17 000000	
	20 000000	
 ERROR MESSAGES BATTERY FAILURE KEYBOARD ECHO RE-ENTER DS PROGRAMS		

Figure C-14. Maintenance Register Display, Page 1

PM WXX YYYYYY (PP Memory)

NOTE

This command causes the PP containing the memory to be displayed to be forced idle. Hence, it may not be used to observe memory during program execution.

The PM command causes 1008 words of PP memory WXX to be displayed on the screen, starting at address YYYYYY (figure C-15). Sequential locations are listed from left to right on each line. The start address of each line is listed to the left of that line for reference. The addresses consist of five octal digits and the data consists of six octal digits. The parameter WXX selects the logical PP memory to be displayed, and may be any octal number in either the range N0 through N11, N20 through N31 or C0 through C11. The parameter YYYYYY may be any octal number in the range 0 through 17777 (0 through 7777 if NIO memory is in 4K mode). Note that if a long deadstart sequence (LDS) was previously interrupted (or hung) without going to completion, then LDS mode will remain set in the PPs. When displaying memory for PP0 in this case, addresses greater than or equal to 6000 will contain the LDS program.

When this display is active, pressing the + or - key (no **Enter**) increments or decrements the PP memory starting address by 1008. If the memory display for a PP of a non-existent barrel is requested, the message BARREL NOT INSTALLED is displayed.

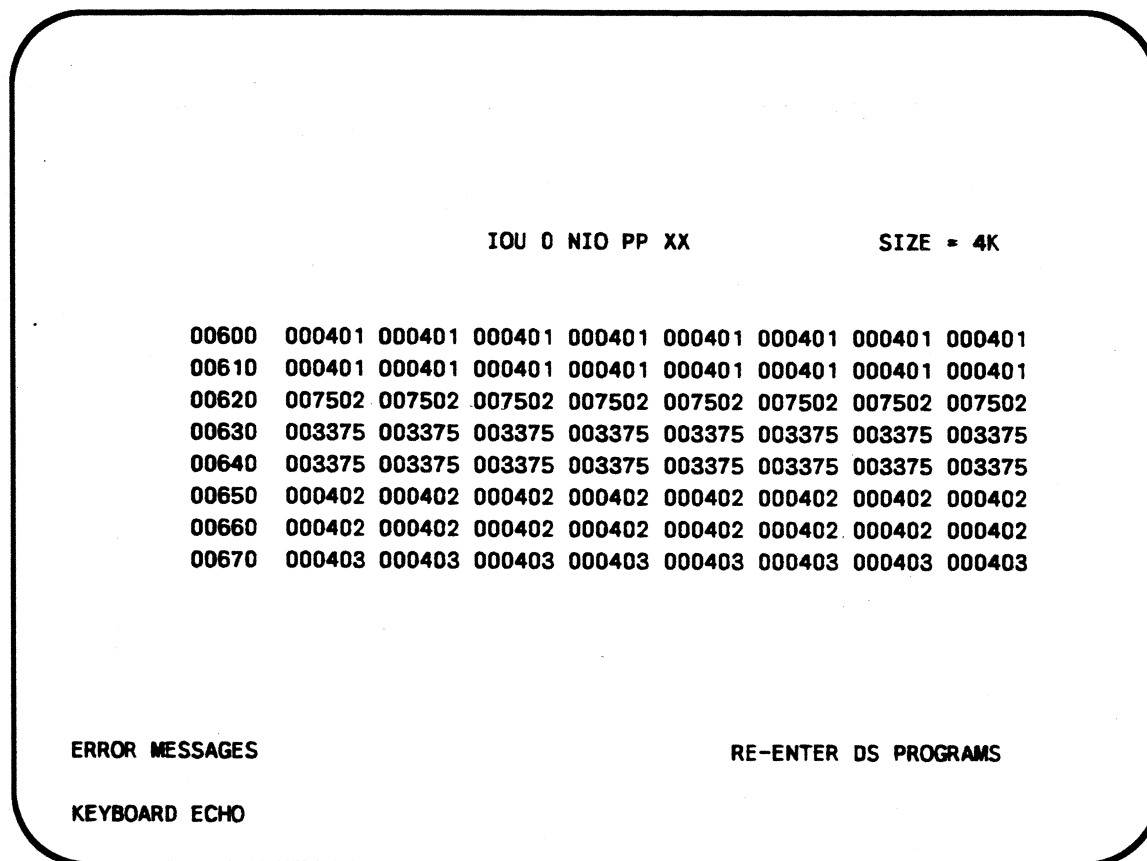


Figure C-15. PP Memory Display

PR WX (PP Register)

This command causes the PP registers, P, A, Q and K, of an NIO or CIO logical barrel to be displayed on the right-hand side of the screen (figure C-16). The logical barrel number is indicated above the display and the logical PP numbers within the barrel are listed in the left column of the display. PPs are numbered in octal and the contents of the P, A, Q, and K registers are also displayed as octal digits. This live display is constantly updated.

When the PR display is active, the + and - key provide a convenient means of selecting the logical barrel to be displayed. Pressing the + key causes the current barrel to be replaced by the next higher numbered logical barrel, with CIO barrels 0 and 1 following NIO barrel 3. If the - key is pressed, the next lower numbered logical barrel replaces the current barrel.

If the registers for a non-existent barrel are requested, the message BARREL NOT INSTALLED is displayed.

MAINTENANCE OPTIONS - IOU 0
MODEL 40 (S/N XXXX) REV. 15

XX YYYYYY-CHANGE DS PRG	PROGRAM 0	+=ADU BUSY	NIO BARREL=0
XX+YYYYYY-CHANGE DS PRG INC	01 000300	*=PP IDLE	EX BUSY=0
S-SHORT DS	02 000000		
L-LONG DS	03 000000	PP P A Q K	
H-HELP	04 000000	*+00 000001 007757 000001 107700	
	05 000000	+01 007777 010000 000001 007100	
	06 000000	* 02 007777 010000 000002 107700	
	07 000000	03 007777 010000 000003 007100	
	10 000000	04 007777 010000 000004 007100	
PPM CONF = 0	11 000000		
NIO BRL CONF = 0	12 000000		
DLY LOOP = 0	13 000000		
LDS ADDR = 6000	14 000000		
CLK FREQ = NORMAL	15 000000		
NIO MEM SIZE = 4K	16 000000	BRANCH TEST FAILURE	
STAT SUM = 14	17 000000	TFR ERR XXXXX YYYYYY (ZZZZZZ)	
	20 000000	STATUS SUMMARY ERROR	
ERROR MESSAGES		BATTERY FAILURE	
KEYBOARD ECHO		RE-ENTER DS PROGRAMS	

Figure C-16. PP Register Display

PS XX YYY (PS Command)

This command is used to turn NIO channel parity error detection circuits on or off. By entering ON for the parameter YYY, the parity switch bit is set to 0, indicating that testing of parity will occur on channel XX. By entering OFF for the parameter YYY, the parity switch bit is set to 1 indicating that parity testing is inhibited on channel XX. The state of this switch is displayed on the NIO Channel Status Display in the DIS PE field.

Note that parity error detection on channels 10, 14, 15 and 17 cannot be turned off.

When the RE-ENTER DS PROGRAMS message is displayed, the password must also be re-entered.

R (Return to Maintenance Options Display)

The R command provides the user with a convenient means of returning to the Maintenance Options Display when desired. This command can also be used to terminate execution of an SD command.

RT (Release Terminals)

This command is supported only on TPMs having revision 14 firmware or later. The RT command causes the TPM microprocessor to release its control of the system console. This allows the software running in the PPs control of the terminal and allows port 0 and port 1 to again respond to functions on channel 15 and the maintenance access control (MAC) circuits.

This command also causes the TPM to release control of channels 10 and 17.

SD (Short Deadstart Display Loop)

This command repeatedly performs short deadstart sequences, with a time between deadstarts corresponding to the delay loop setting (see DE X command). Between sequences, it updates the display currently up. Changes may be made to the deadstart program while the display loop is running by using the command XX YYYYYY. Alternatively, the command TB XX YYYYYY may be used to repeatedly toggle selected bits in the deadstart program. These features allow the person troubleshooting the machine to "try out" various test operands and observe the effect of these operands on the hardware by looking at the current display. Thus, it is easy to identify "stuck-at-one" and "stuck-at-zero" hardware faults. In addition, while the SD command is running, new displays can be selected. Note, however, that the SM and SS commands may not be used with SD.

The following actions terminate the execution of the SD command:

- Executing the R command (the recommended termination method).
- Executing any of the commands S, L, RT, QUIT, H, D, DT, *T, or *R.
- Activating the Deadstart Options Display or the Maintenance Options Display.

SM (Scope Mode)

The purpose of scope mode is to allow the use of an oscilloscope in troubleshooting the hardware involved in various deadstart display commands. The SM command prepares the TPM microprocessor to enter a tight loop on the next command, which may be any of the following.

- S The short deadstart program is executed repeatedly in its entirety. The TB (Toggle Bit) and the DE (Delay) features may be used.
- L The LDS program is executed repeatedly starting at the address specified by LDS ADDR=XXXX. The LA command may be used to alter this address from the initialized value of 6000, but care must be taken when choosing a different address to ensure that a valid entry point is selected. In contrast to using the short deadstart command, entering L following an SM command causes the LDS program to be loaded into PP memory only once. In the case of the S command, the short deadstart program is loaded into PP memory each time the program is executed. The DE (delay) feature may also be used.
- RP Repeatedly loads the physical PP number declared to be logical PP 0 into the hardware reconfiguration register. The existing RB value is loaded at the same time.
- RB Repeatedly loads the physical barrel number declared to be logical barrel 0 into the hardware reconfiguration register. The existing RP value is loaded at the same time.
- PR Repeatedly reads the P, A, Q and K registers for the first logical PP in the selected barrel.
- PM Repeatedly reads eight words of PP memory beginning at address YYYYYY of PP WXX.
- EP Repeatedly writes data YYYYYYY into address XXXXX of the PP memory being displayed at the time the scope loop was entered.
- MR Repeatedly reads PP maintenance register 12₁₆ (only).
- ER Repeatedly reads and writes eight bytes of data into byte Y of maintenance register XX₁₆. The read and write data is identical except for byte Y.
- CH Repeatedly reads 28 status bytes for NIO channels.
Or repeatedly reads 10 status bytes for CIO channels.
- FI Repeatedly issues an idle to PP WXX.
- CF Repeatedly writes and reads the clock frequency register.
- PS Repeatedly writes channel status bytes with only channel XX parity bit changed.
- CL Repeatedly clears the IOU LEDs.
- DC Repeatedly deadstarts channel WXX.
- DS Repeatedly loads the short deadstart program and issues a deadstart master clear.

MC Repeatedly master clears the ADU and clears IOU errors.

SS Repeatedly reads the status summary register.

During scope mode operation, the console display is not refreshed and no further commands are accepted. Typing **Ctrl-G** followed by **Ctrl-R** on a terminal connected to a TPM port are the only ways to exit scope mode.

TB XX YYYYYY (Toggle Bit)

This command is used to automatically toggle selected bits in the deadstart program. Parameter YYYYYY is a string of 1 through 6 octal digits and is used as a mask to select the bits to be toggled: binary 1's in this parameter cause corresponding bits to be toggled in word XX.

The TB command is intended to be used in conjunction with the SD command or with the S command in scope mode. The selected bits are toggled during each repetition of a loop. Once this feature is selected, it may be deactivated only by typing **Ctrl-G** and then re-activating the Maintenance Options Display on the same IOU. Toggle time may be adjusted using the DE command.

XM XXX (Extended PP Memory ON/OFF)

This command may be used to select between 4K (normal) and 8K (extended) PP memory modes. ON selects 8K mode, OFF selects 4K mode. Executing either a short deadstart or a long deadstart resets the mode to normal.

***R (Power-On Reset)**

NOTE

This command destroys the contents of the deadstart program words 0 through 3 and clears the calendar clock.

The *R command resets the TPM deadstart parameters without the need to cycle system power after the battery has failed. After executing *R, the Maintenance Options Display appears with the message RE-ENTER DS PROGRAMS.

***SYMMDDHHMM (Set Time)**

***SYMMDDHHMM (Set Time)**

This command is used to set the calendar/clock provided the Calendar/Clock Display (figure C-17) is active, this command may be used to set the calendar/clock. The clock should be set using a consecutive 24 hour time period (military time) as follows:

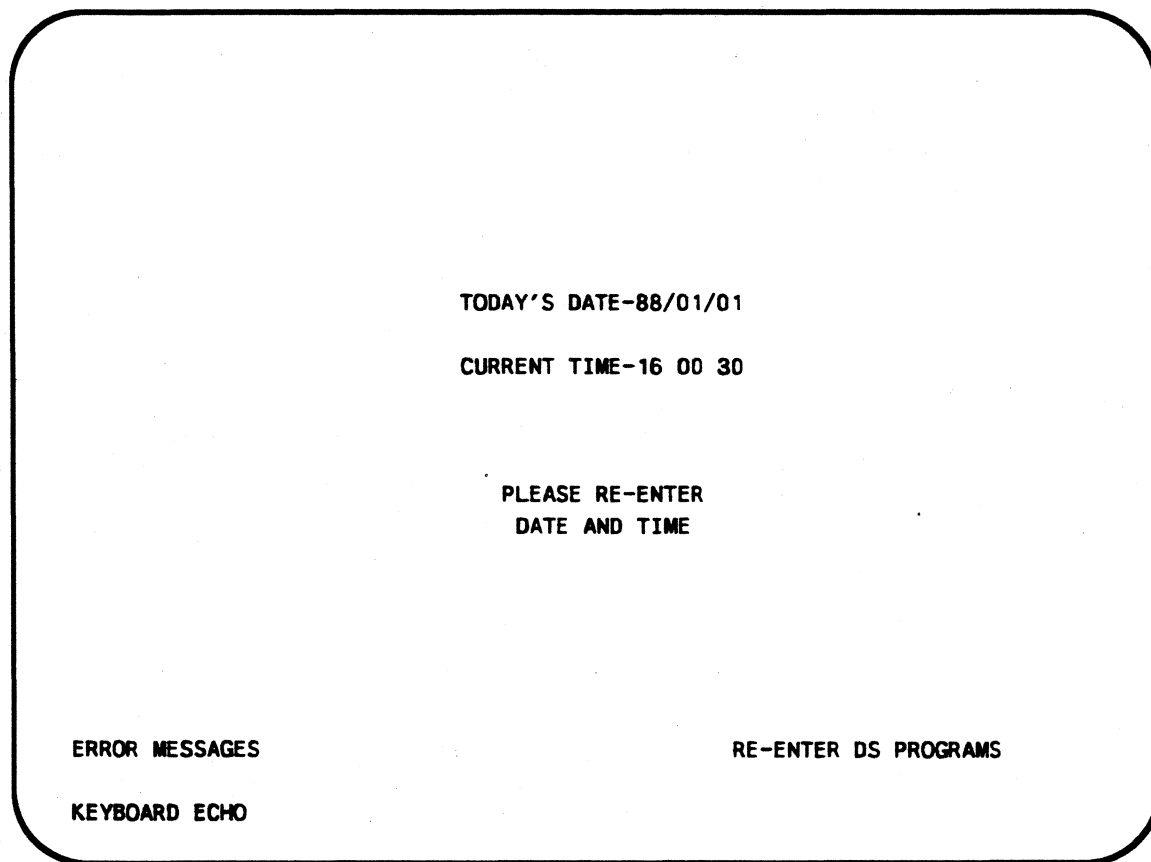
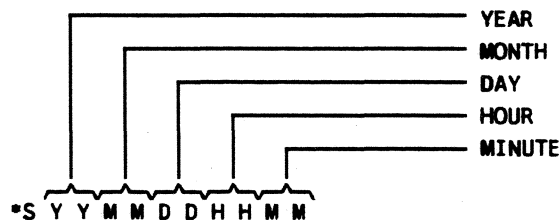


Figure C-17. Calendar/Clock Display

*T (Display Time)

This command causes the Calendar/Clock Display (figure C-17) to appear. If the calendar/clock needs to be set, the message PLEASE RE-ENTER DATE AND TIME appears.

Miscellaneous Keyboard Entries

The following keyboard entries are used to perform various command functions as indicated.

Enter	Terminates all commands except +, -, and space bar .
Backspace	Deletes the last character entered and removes the keyboard error message if present.
Delete	Deletes the complete keyboard entry line and removes the keyboard error message if present.
Esc	Deletes the complete keyboard entry line and removes the keyboard error message if present.

Battery or RAM Failure

The TPM contains a lithium battery that maintains deadstart programs 0 through 3 and the reconfiguration status, and also allows the calendar/clock to continue running with line power removed. A fresh battery will support these functions for at least 4000 hours.

If line power (50/60 Hz) is removed long enough to deplete the battery charge or if the 1JKH module is removed from the IOU, the loss of data is sensed and the following action is taken when power is re-applied:

- Deadstart programs 0 through 3 are erased and replaced with a 000300 in word 1 and zeros in all remaining words.
- Reconfiguration and other parameters are set to default values.
- The time-of-day is erased, and a status bit is set for software to indicate a loss of time data.
- When **Ctrl-G** then **Ctrl-R** are pressed, the Maintenance Options Display is brought up instead of the Deadstart Options Display. The following messages are also displayed:

```
BATTERY FAILURE
RE-ENTER DS PROGRAMS
```

These messages are removed when the first entry is typed into the deadstart program on the screen.

When a TPM RAM failure is detected, the same actions are taken except that the message displayed will be:

```
RE-ENTER DS PROGRAMS
```

Two-Port Mux Internal Diagnostic (D) Tests

The internal diagnostic tests are a feature of the TPM microprocessor firmware that provide a quick check on IOU deadstart-related hardware. These tests include scope loops to aid in troubleshooting the problems the tests uncover.

The internal diagnostic tests may be executed using either with the D or DT WX commands, where W must be either N for NIO, or C for CIO. The parameter X corresponds to a test number and can be any number from 0 to 7 for NIO tests, or from 2 to 6 for CIO tests. Command D causes the tests to execute one after the other beginning with NIO test 0. Command DT WX causes execution to begin at either the NIO or CIO version of test X. Since the CIO version of a particular test always runs after the NIO version, when execution begins with the CIO version the NIO version is not executed.

Either command, D or DT WX, causes the Diagnostic Display shown in figure C-18 to appear on the screen. If both the NIO and CIO versions of a particular test finish without errors, the message OK appears on the screen opposite the test name. The message FAULT appears if either the CIO or NIO version of a test detects an error.

If an error is detected, the Diagnostic Display is replaced by an error message identifying the test, the failing data, and the IOU modules that could be responsible for the error. See figures C-18 through C-26 for error display examples. After the error message has appeared, the SM command can be used to enable the failing test's scope loop. Pressing the - key causes the TPM microprocessor to begin executing the loop.

If no scope loop is desired after an error, pressing the - key without first entering the SM command causes the same test to begin executing with the next test data pattern. A + entry skips the rest of the current test and executes the remaining tests.

All tests, with the exception of test 0 and 1, destroy the previous contents of the maintenance registers, the P, A, K and Q PP registers, and logical PP memory 0. Table C-2 describes the internal diagnostic tests.

Table C-1. Internal Diagnostic Tests

Number	Test	Description
0	TPM RAM	Writes and reads the TPM RAM at addresses 5000 through 53FF ₈ . If no error stop occurs, the original content of the test location is preserved. The test pattern is 0 through FF ₁₆ increment by 1.
1	MAC Echo	Tests the MAC maintenance channel interface by echoing back the test pattern 0 through FF ₁₆ increment by 1.
2	OS Bounds Register	Tests the MAC interface by writing and reading byte 6 of this register. The test pattern is 0 through FF ₁₆ increment by 1.
3	BAS 0 PP Register	Initializes the P register to 7777 ₈ , the A register to 010000 ₈ , and the K register to 007100 ₈ . The Q register channel number corresponds to the PP number.
4	FS Mask Register	Tests the MAC interface by writing and reading byte 6 of this register. The test pattern is 0 through FF ₁₆ increment by 1.
5	PPM 0 Test Part 1 (Data)	Writes and reads the 4K PP0 memory locations. The test pattern is 0 through 7777 ₈ increment by 401 ₈ .
6	PPM 0 Test Part 2 (Adrs)	Writes one location and checks that it has not written elsewhere. The test pattern is 125252 ₈ constant write to 0 through 4000 ₈ increment by left circular shift.

MAINTENANCE OPTIONS - IOU 0		
MODEL 40 (S/N XXXX) REV. 15		
XX YYYYYY-CHANGE DS PRG	PROGRAM 0	
XX+YYYYYY-CHANGE DS PRG INC	01 000300	
S-SHORT DS	02 000000	
L-LONG DS	03 000000	DIAGNOSTICS
H-HELP	04 000000	
	05 000000	
	06 000000	0)TPM RAM TEST.....OK
	07 000000	1)MAC ECHO TEST.....OK
PPM CONF = 0	10 000000	2)OS BOUNDS REGISTER TEST...FAULT
NIO BRL CONF = 0	11 000000	3)BAS 0 PP REGISTER TEST...OK
DLY LOOP = 0	12 000000	4)FS MASK REGISTER TEST....OK
LDS ADDR = 6000	13 000000	5)PPM 0 TEST PART 1(DATA)...RUNNING
CLK FREQ = NORMAL	14 000000	6)PPM 0 TEST PART 2(ADDR)...
NIO MEM SIZE = 4K	15 000000	7)4K/8K MEM SELECT TEST.....
STAT SUM = 00	16 000000	
	17 000000	
	20 000000	
ERROR MESSAGES		BATTERY FAILURE
KEYBOARD ECHO		RE-ENTER DS PROGRAMS

Figure C-18. Internal Diagnostic Test Display (Test in Process)

MAINTENANCE OPTIONS - IOU 0		
MODEL 40 (S/N XXXX) REV. 15		
XX YYYYYY-CHANGE DS PRG	PROGRAM 0	
XX+YYYYYY-CHANGE DS PRG INC	01 000300	
S-SHORT DS	02 000000	
L-LONG DS	03 000000	DIAGNOSTICS
H-HELP	04 000000	
	05 000000	
	06 000000	
	07 000000	TPM RAM ADDR.C007 EXP.01 REC.FF
PPM CONF = 0	10 000000	
NIO BRL CONF = 0	11 000000	SUSPECTED FAILING PAKS
DLY LOOP = 0	12 000000	1JKH B23
LDS ADDR = 6000	13 000000	
CLK FREQ = NORMAL	14 000000	
NIO MEM SIZE = 4K	15 000000	
STAT SUM = 00	16 000000	
	17 000000	
	20 000000	
ERROR MESSAGES		BATTERY FAILURE
KEYBOARD ECHO		RE-ENTER DS PROGRAMS

Figure C-19. Diagnostic Display, TPM RAM Test Error Message

MAINTENANCE OPTIONS - IOU 0			
MODEL 40 (S/N XXXX) REV. 15			
XX YYYYYY-CHANGE DS PRG	PROGRAM 0		
XX+YYYYYY-CHANGE DS PRG INC	01 000300		
S-SHORT DS	02 000000		
L-LONG DS	03 000000	DIAGNOSTICS	
H-HELP	04 000000		
	05 000000		
	06 000000		
	07 000000	MAC ECHO	EXP.01 REC.FF
PPM CONF = 0	10 000000		
NIO BRL CONF = 0	11 000000	SUSPECTED FAILING PAKS	
DLY LOOP = 0	12 000000	1JQH A22	
LDS ADDR = 6000	13 000000	1JKH B23	
CLK FREQ = NORMAL	14 000000	1JAH A01	
NIO MEM SIZE = 4K	15 000000		
STAT SUM = 00	16 000000		
	17 000000		
	20 000000		
ERROR MESSAGES		BATTERY FAILURE	
KEYBOARD ECHO		RE-ENTER DS PROGRAMS	

Figure C-20. Diagnostic Test Display, MAC Echo Test Error Message

MAINTENANCE OPTIONS - IOU 0			
MODEL 40 (S/N XXXX) REV. 15			
XX YYYYYY-CHANGE DS PRG	PROGRAM 0		
XX+YYYYYY-CHANGE DS PRG INC	01 000300		
S-SHORT DS	02 000000		
L-LONG DS	03 000000	DIAGNOSTICS	
H-HELP	04 000000		
	05 000000		
	06 000000		
	07 000000	NIO OS(BYTE 0)	EXP.01 REC.1F
PPM CONF = 0	10 000000		
NIO BRL CONF = 0	11 000000	SUSPECTED FAILING PAKS	
DLY LOOP = 0	12 000000	1JCH A11	
LDS ADDR = 6000	13 000000	1JQH A22	
CLK FREQ = NORMAL	14 000000	1JXH B23	
NIO MEM SIZE = 4K	15 000000	1JAH A01	
STAT SUM = 00	16 000000		
	17 000000		
	20 000000		
ERROR MESSAGES		BATTERY FAILURE	
KEYBOARD ECHO		RE-ENTER DS PROGRAMS	

Figure C-21. Diagnostic Display, OS Bounds Register Test Error Message

```

MAINTENANCE OPTIONS - IOU 0
MODEL 40 (S/N XXXX) REV. 15

XX YYYYYY-CHANGE DS PRG          PPM CONF = 0
XX+YYYYYY-CHANGE DS PRG INC      NIO BRL CONF = 0
S-SHORT DS                       DLY LOOP = 0
L-LONG DS                        LDS ADDR = 6000
H-HELP                           CHK FREQ = NORMAL
                                NIO MEM SIZE = 4K
                                STAT SUM = 00

PROGRAM 3

01 000300          DIAGNOSTICS
02 000000          PP  P   A   Q   K   NIO
03 000000          00 007777 010000 000000 007100 EXP.
04 000000          00 000000 000000 000000 000000 REC.
05 000000          SUSPECTED FAILING PAKS
06 000000
07 000000          1JCH  A11
10 000000
11 000000          1JQH  A22
12 000000
13 000000          1KRH  B15
14 000000
15 000000          1JTH  A21
16 000000
17 000000
20 000000
ERROR MESSAGES          BATTERY FAILURE
KEYBOARD ECHO           RE-ENTER DS PROGRAMS

```

Figure C-22. Diagnostic Display, PP Register Test Error Message

MAINTENANCE OPTIONS - IOU 0			
MODEL 40 (S/N XXXX) REV. 15			
XX YYYYYY-CHANGE DS PRG	PROGRAM 0		
XX+YYYYYY-CHANGE DS PRG INC	01 000300		
S-SHORT DS	02 000000		
L-LONG DS	03 000000	DIAGNOSTICS	
H-HELP	04 000000		
	05 000000		
	06 000000		
	07 000000	NIO MASK(BYTE4) EXP.01 REC.FF	
PPM CONF = 0	10 000000		
NIO BRL CONF = 0	11 000000	SUSPECTED FAILING PAKS	
DLY LOOP = 0	12 000000	1JTH A21	
LDS ADDR = 6000	13 000000	1JQH A22	
CLK FREQ = NORMAL	14 000000	1JXH B23	
NIO MEM SIZE = 4K	15 000000	1JAH A01	
STAT SUM = 00	16 000000		
	17 000000		
	20 000000		
ERROR MESSAGES		BATTERY FAILURE	
KEYBOARD ECHO		RE-ENTER DS PROGRAMS	

Figure C-23. Diagnostic Display, Fault Status Mask Register Test Error Message

MAINTENANCE OPTIONS - IOU 0		
MODEL 40 (S/N XXXX) REV. 15		
XX YYYYYY-CHANGE DS PRG	PROGRAM 0	
XX+YYYYYY-CHANGE DS PRG INC	01 000300	
S-SHORT DS	02 000000	
L-LONG DS	03 000000	DIAGNOSTICS
H-HELP	04 000000	
	05 000000	
	06 000000	
	07 000000	NIO MASK(BYTE4) EXP.01 REC.FF
PPM CONF = 0	10 000000	
NIO BRL CONF = 0	11 000000	SUSPECTED FAILING PAKS
DLY LOOP = 0	12 000000	1JTH A21
LDS ADDR = 6000	13 000000	1JQH A22
CLK FREQ = NORMAL	14 000000	1JKH B23
NIO MEM SIZE = 4K	15 000000	1JAH A01
STAT SUM = 00	16 000000	
	17 000000	
	20 000000	
ERROR MESSAGES		BATTERY FAILURE
KEYBOARD ECHO		RE-ENTER DS PROGRAMS

Figure C-24. Diagnostic Display, PP Memory Data Test Error Message

MAINTENANCE OPTIONS - IOU 0			
MODEL 40 (S/N XXXX) REV. 15			
XX YYYYYY-CHANGE DS PRG	PROGRAM 0		
XX+YYYYYY-CHANGE DS PRG INC	01 000300		
S-SHORT DS	02 000000		
L-LONG DS	03 000000	DIAGNOSTICS	
H-HELP	04 000000		
	05 000000		
	06 000000	PART 2 ADDR. EXP. REC.	
	07 000000	NIO PPM 00001 000001 000000	
	10 000000		
PPM CONF = 0	11 000000	SUSPECTED FAILING PAKS	
NIO BRL CONF = 0	12 000000	1JCH A11	
DLY LOOP = 0	13 000000	1JSH A20	
LDS ADDR = 6000	14 000000	1KRH B15	
CLK FREQ = NORMAL	15 000000	1KBH B28	
NIO MEM SIZE = 4K	16 000000	1JWH B14	
STAT SUM = 00	17 000000		
	20 000000		
ERROR MESSAGES		BATTERY FAILURE	
KEYBOARD ECHO		RE-ENTER DS PROGRAMS	

Figure C-25. Diagnostic Display, PP Memory Address Test Error Message

MAINTENANCE OPTIONS - IOU 0			
MODEL 40 (S/N XXXX) REV. 15			
XX YYYYYY-CHANGE DS PRG	PROGRAM 0		
XX+YYYYYY-CHANGE DS PRG INC	01 000300		
S-SHORT DS	02 000000		
L-LONG DS	03 000000	DIAGNOSTICS	
H-HELP	04 000000		
	05 000000		
	06 000000	8KWR-4KRD ADDR. EXP. REC.	
	07 000000	NIO 4/8K 00001 000001 000000	
	10 000000		
PPM CONF = 0	11 000000	SUSPECTED FAILING PAKS	
NIO BRL CONF = 0	12 000000	1JCH A11	
DLY LOOP = 0	13 000000	1JSH A20	
LDS ADDR = 6000	14 000000	1KRH B15	
CLK FREQ = NORMAL	15 000000	1KBH B28	
NIO MEM SIZE = 4K	16 000000	1JTH A21	
STAT SUM = 00	17 000000		
	20 000000		
ERROR MESSAGES		BATTERY FAILURE	
KEYBOARD ECHO		RE-ENTER DS PROGRAMS	

Figure C-26. Diagnostic Display, 4K - 8K Memory Select Test Error Message

Deadstart Display Commands Quick Reference Table

Table C-3 contains a listing of the various deadstart display commands that apply to the IOU.

Table C-2. Quick Reference Table

Command	Description
CF X ¹	Enter clock frequency X = F (fast), N (normal), or S (slow) (default = normal)
CH W ¹	PP Channel Status Display (W = N for NIO, or C for CIO)
CL ¹	Clear IOU error LEDs
DC WXX ¹	Deadstart channel (WXX = N0 through N13, N20 through N33, or C0 through C11)
D	Run the complete set of TPM internal diagnostics
DE X ¹	Enter the loop delay value (0 through 7) (default = 0)
DS ¹	Issue a deadstart master clear, execute the short deadstart program, momentarily release channels 10 and 17, then return to the current display
DT WX	Run the TPM internal diagnostics starting at test WX
EM XXXXX YYYYY ZZZZZ ¹	Enter data pattern ZZZZZ into PP memory starting address XXXXX to ending address YYYYY. (If PP Memory Display is up.)
EP XXXXX YYYYYY ¹	Enter data YYYYYY into PP memory location XXXXX (If PP memory display is up.)
EP+XXXXX YYYYYY ¹	Same as above, plus increment address
ER XX Y ZZ ¹	Enter data ZZ (hex) into byte Y of maintenance register XX (hex) (If the Maintenance Register Display is up.)
ER+XX Y ZZ ¹	Same as above, plus increment byte number
FI WXX ¹	Idle PP (WXX = PP number N0 through N11, N20 through N31, or C0 through C11)
GP X ¹	Get deadstart program X (0 through 7) (default = program 0)

Note:

1. This command also appears on the Help display.

(Continued)

Table C-2. Quick Reference Table (Continued)

Command	Description
(space bar) ¹	Get the next deadstart program
H	Help Display
I ¹	Initialize the IOU
L	Long deadstart
LA YYYY ¹	Enter octal long deadstart starting address (default = 6000)
MC ¹	Clear errors and master clear the ADU
MP WXX WYY ¹	Move whole PP memory XX to PP memory YY (W = N for NIO, or C for CIO)
MR ¹	PP Maintenance Register Display
PM WXX YYYYY ¹	PP Memory Display (WXX = PP number N0 through N11, N20 through N31, or C0 through C11; YYYYY = starting address)
PR WX ¹	PP Register Display (WX = barrel N0 through N3, or C0 through C1)
PS XX YYY ¹	Enter NIO channel XX parity error switch YYY = ON or OFF (ON enables parity error detection.) (Default = ON)
R ¹	Return to the Maintenance Options Display
RB X ¹	Enter NIO barrel configuration number (0 through 3) (default = 0)
RP X ¹	Enter PP configuration number (0 through 4) (default = 0)
RT	Release terminal
S	Short deadstart
SD ¹	Short deadstart display loop
SM	Arm the scope mode for the following commands: S, L, RP, RB, PR, PM, EP, MR, ER, CH, FI, CF, PS, CL, DC, D, DT, DS, XM, MC, and SS

Note:

1. This command also appears on the Help display.

(Continued)

Table C-2. Quick Reference Table *(Continued)*

Command	Description
SP X ¹	Save the screen deadstart program as PROGRAM X (0 through 3)
SS	Status summary scope loop (if scope mode is armed)
TB XX YYYYYY ¹	Toggle bits YYYYYY in word XX (initialized every deadstart to word 01, no bits toggled)
XM XXX ¹	Extend NIO memory size XXX=ON(8K) or OFF(4K) (default = OFF)
XX YYYYYY	Enter deadstart program data
XX+YYYYYY	Enter deadstart program data and increment to the next deadstart program address
*R	Power-on reset
*SYMMDDHHMM	Set calendar clock time if displayed (Initialized with months, days, hours, and minutes = 0, years = 85 and status bad.)
*T	Display calendar clock time
+	Increment barrels (if the PR display is on) Toggle between NIO and CIO displays (if the CH display is on) Toggle between page 1 and page 2 displays (if either the Help or MR display is on) Display the next 1008 PP memory words (if the PM display is on) Advance to the next internal diagnostic test (if a diagnostics error display is on)
-	Decrement barrels (if the PR display is on) Display the previous 1008 PP memory words (if the PM display is on) Advance to the next test pattern in current internal diagnostics test (if a diagnostics error display is on)

Note:

1. This command also appears on the Help display.

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The deadstart display features described in this appendix include commands and associated displays for deadstarting the system and for performing basic maintenance functions in the IOU. The commands may be entered by the user at the keyboard of the system console. The deadstart display features are supported via the program memory of the two-port multiplexer (TPM) microprocessor contained in the IOU; it is not necessary for a program to be operational in the PPs.

Hardware Interface

The TPM provides two RS-232-C interfaces called port 0 and port 1. During normal operation, each port provides an interface between the operating system via channel 15 and the system console. In this mode, the display on the screen of the console and the interpretation of the commands entered at the console's keyboard are under the control of the software running in the PPs.

However, in order to support the deadstart display features, the TPM microprocessor must first exit this mode. This is accomplished by using a **Ctrl-G, Ctrl-R** sequence as described under Software Interface. During this sequence, channel 15 loses its control over the RS-232-C ports and does not regain control again until the sequence is aborted, or a short deadstart, long deadstart, or release terminals (RT) command is executed.

The **Ctrl-G, Ctrl-R** sequence also causes channel 17 (the maintenance access channel) to become unavailable to the PPs. It becomes available again only if the sequence is aborted, or a short deadstart, long deadstart, or RT command is executed.

NOTE

It is possible to use the deadstart display on either port to inspect internal data on a running system with the following restrictions:

- Any PP attempting to use channel 17 (the maintenance access channel) will hang.
- The software currently running in the PPs must not attempt to use channel 15 TPM or calendar/clock features.
- The following displays and commands are potentially destructive:
 - PP Memory Display (PM)
 - Maintenance Register Display (MR)
 - Enter PP Memory Command (EP)
 - Enter Maintenance Register Command (ER)
 - Any of the commands used to reconfigure, idle, or deadstart

Software Interface

The Console Main Menu is activated by typing **Ctrl-G** (e.g., press the **G** key while holding down the **Ctrl** key) or **Ctrl-F2** at the console keyboard. This key sequence causes the system console to clear the screen and paint the Console Main Menu as shown in figure D-1 (this has no effect on the TPM microprocessor, channel 15 or channel 17). Once this display is on the screen, the user may select one of the three options **S** (System Load Options), **M** (Maintenance Options), or **C** (Console Utilities).

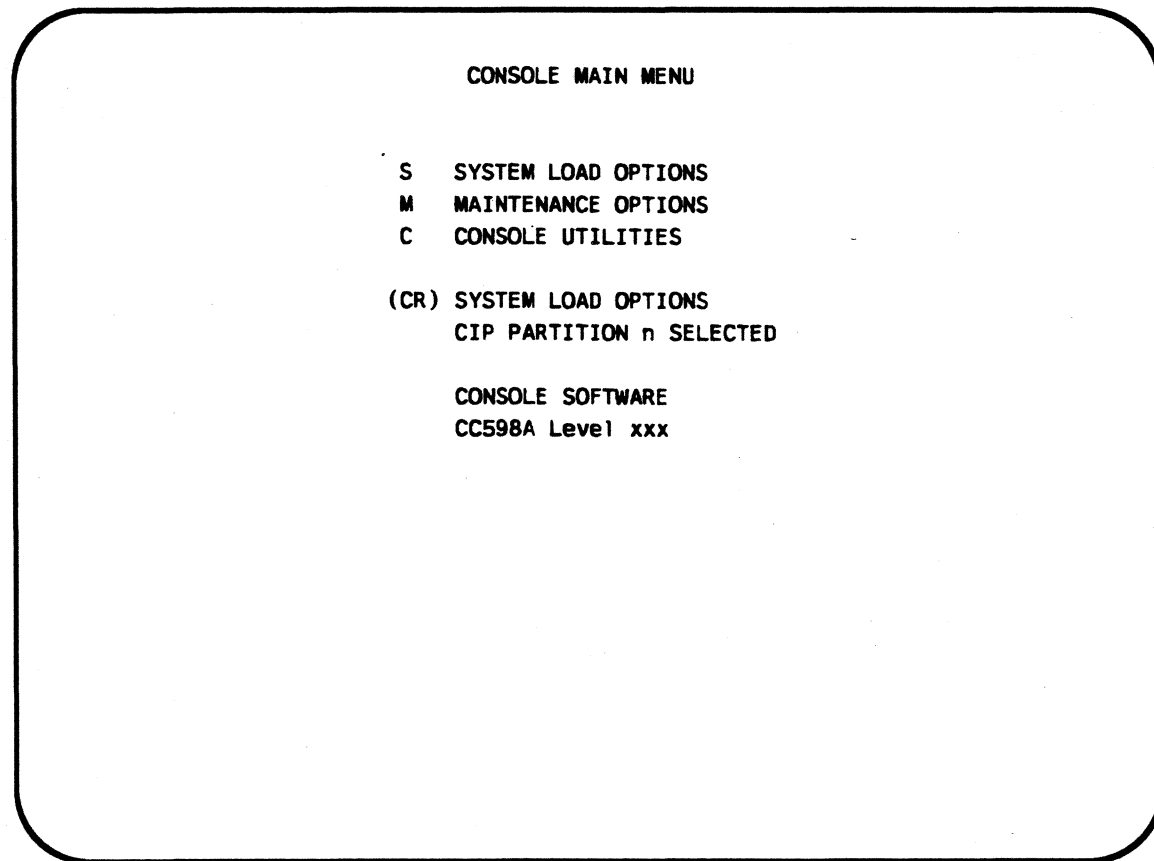


Figure D-1. Console Main Menu

When **M** (Maintenance Options) is selected, the Maintenance Options Display shown in figure D-2 appears. The user can then advance to the IOU-0 Maintenance Options Display by typing **0**, or to the IOU-1 Maintenance Options Display by typing **1**. A selection is also available to perform a system load with a long deadstart by typing **L**.

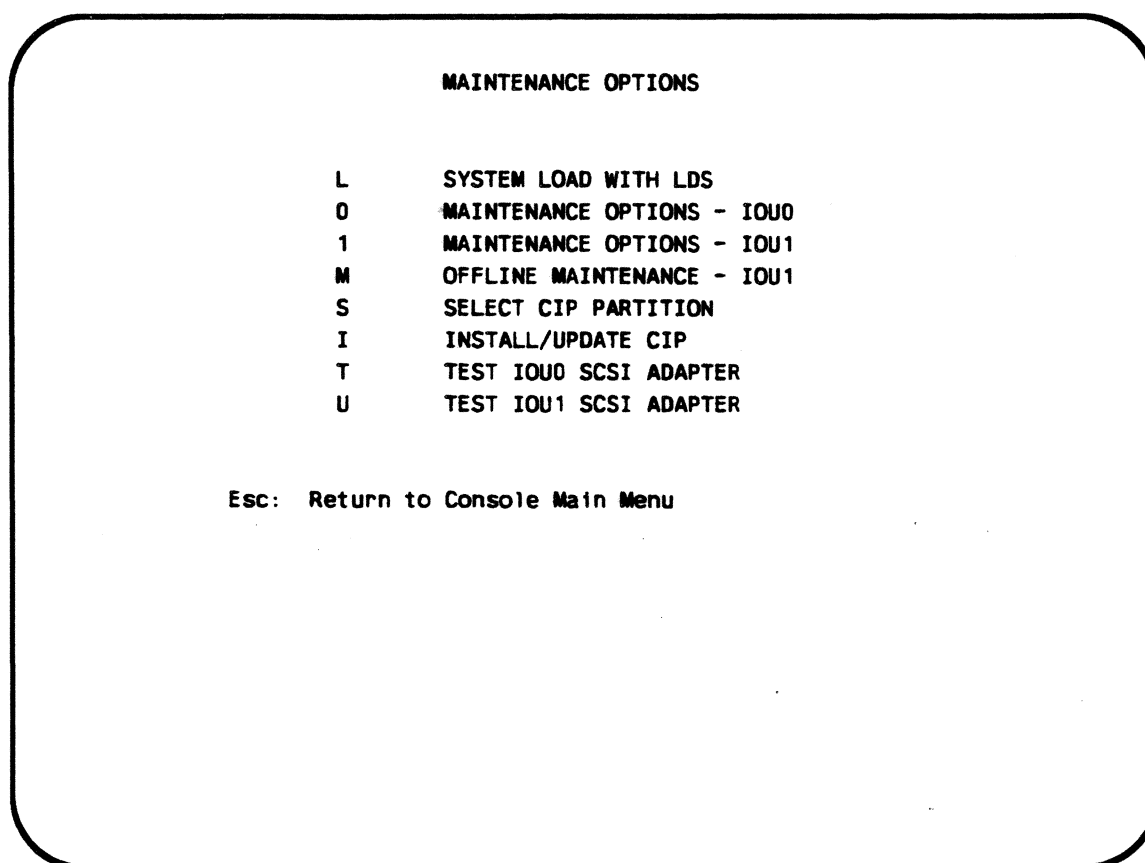


Figure D-2. Maintenance Options Display

IOU Maintenance Options Display

The IOU Maintenance Options Display is shown in figure D-3. When this display is active, the user has access to all of the deadstart display features described in this appendix.

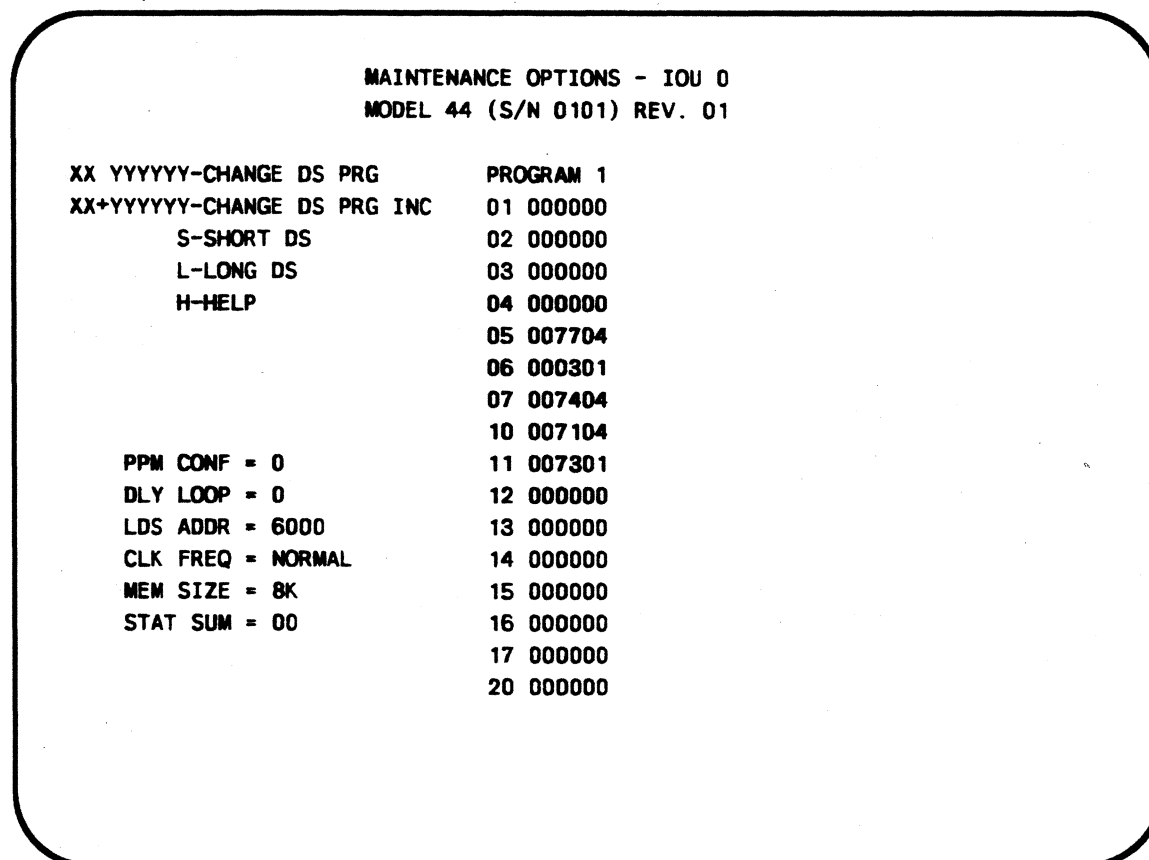


Figure D-3. IOU Maintenance Options Display

The IOU Maintenance Options Display (figure D-3) contains the following information:

- The IOU number: 0 = primary IOU, 1 = secondary IOU.
- The revision number of the TPM microprocessor firmware.
- A 16-word deadstart program for PP0. The words in the program are numbered sequentially from 18 to 208, and each word contains six octal digits.
- A list of some basic keyboard commands and their functions for reference (XX YYYYYY, XX+YYYYYY, S, L, and H). (Refer to Editing Deadstart Programs described later in this appendix for usage of commands XX YYYYYY and XX+YYYYYY. Refer to Deadstarting the PPs for descriptions of the S and L commands. Refer to figures D-4 and D-5 for the contents of the Help displays available, or enter H followed by a Return to view them on the display screen.)
- Reconfiguration status for PP memories.

The line PPM CONF = X indicates the current reconfiguration status of the PP memories. The number X is in the range 0 through 4, and is the number of the physical PP memory which is being used as logical PP0 memory.

- DLY LOOP indicates the delay loop value (0 through 7) for long scope loops (L, S, and SD).
- LDS ADDR indicates the program starting address for a long deadstart sequence.
- CLK FREQ indicates the system clock speed (fast, normal, or slow).
- MEM SIZE = XK indicates the memory size, where XK is 4K or 8K, indicates what size PP memory is set at.
- SUM STAT = XX indicates an 8-bit summary status byte of various IOU error conditions. (Refer to appendix B for error code definitions.)
- A battery failure line - displayed on the lower right-hand side of the screen, it indicates that short deadstart sequence (SDS) programs and initial configurations must be re-entered.
- A keyboard entry line - the bottom line of the display is used to echo back the entries made by the operator on the keyboard of the console. With acceptance of a valid command, the keyboard entry is erased.
- An error line - the line immediately above the keyboard entry line is used to indicate that the keyboard entry has an error in it. Pressing the Backspace, Escape, or Delete keys removes this line.
- LDS status - if a long deadstart sequence aborts because of a hardware malfunction, the type of error is displayed on the lower right-hand side of the screen. Possible errors are:
 - LDS BRANCH TEST FAILURE
 - LDS PROGRAM TRANSFER ERROR
 - STATUS SUMMARY ERROR (for IOU errors only)
- PP registers: the contents of the P, A, Q, and K registers for the PPs in the deadstart barrel may be displayed on the right-hand side of the screen. This display is brought up automatically during a long deadstart, but may also be brought up by using the maintenance command PR.

HELP Displays

Figures D-4 and D-5 show the contents of the two Help displays that are available to the user. These figures list the various commands and their definitions that can be input from the keyboard. For example: Type H followed by **Enter** to view Help Display, Page 0 on the console screen. Press + (**Enter**) to toggle to Help Display, Page 1. Type R (**Enter**) to return to the IOU Maintenance Options Display.

HELP DISPLAY	
R	RETURN TO MAINT OPTIONS DISPLAY
I	INITIALIZE IOU
GP X	GET DS PRG 0-7
	RAM USER PRG 0-3
SPACE BAR	SELECT NEXT DS PRG
SP X	STORE TO DS PRG 0-3
TB XX YYYYYY	TOGGLE BITS YYYYYY IN DS WORD XX
SD	SHORT DS DISPLAY LOOP
DE X	SET LOOP DELAY 0-7
SM	ARM SCOPE MODE
CH	PP CHAN STATUS DISPLAY
DC XX	DS CH 00-13 OR 20-33
CL	CLEAR LEDS
DS	ISSUE SDS/MC AND KEEP DISPLAY
MC	CLEAR ADU AND CLEAR ERRORS
CF X	SET CLOCK FREQ F,N OR S
SS	STATUS SUMMARY LOOP AFTER SM
(TYPE + TO TOGGLE)	

Figure D-4. Help Display, Page 0

HELP DISPLAY

RP X	SET PP MEM CONFIG 0-4
LA YYYY	SET LDS START ADDR
XM XXX	EXTEND IOU MEM SIZE ON/OFF(8K/4K)
PM XX YYYY	DISPLAY PPM XX STARTING YYYY
+	INC PPM ADDR
-	DEC PPM ADDR
EP XXXXX YYYYYY	ENTER DATA YYYYYY IN PPM LOC XXXXX
EP+XXXXX YYYYYY	AS ABOVE BUT INC ADDR
EM XXXXX YYYYY ZZZZZ	PPM PATTERN ZZZZZ AT XXXXX TO YYYYY
MP XX YY	MOVE PPM FROM PP N/C XX TO PP YY
PR X	PP REG DISPLAY BRL X
+(-)	INC(DEC) LOGICAL BRL FOR REG DISPLAY
FI XX	IDLE PP XX
MR	PP MAINT REG DISPLAY
+	TOGGLE MAINT REG DISPLAYS
ER XX Y ZZ	ENTER HEX DATA ZZ, BYTE Y, MAINT REG XX
ER+ZZ Y ZZ	AS ABOVE BUT INC ADDR
D	B DIAGNOSTIC TESTS STARTING WITH 0
DT X	DIAGNOSTIC TESTS STARTING WITH X

(TYPE + TO TOGGLE)

Figure D-5. Help Display, Page 1

To present the information in this chapter in a structured format, this page has been left blank.

Deadstarting the PPs

There are two basic commands provided to deadstart the PPs: S and L. Command S is used to initiate a short deadstart sequence. Command L is used to initiate a long deadstart sequence. These commands are described in the following paragraphs.

Command S

Command S (followed by **Enter**) is used to initiate a short deadstart sequence. In this sequence, a deadstart master clear is issued to the PPs and I/O channels and the program currently being displayed on the screen is loaded into logical PP0. Execution begins at word 1 of this program. At the end of the sequence, the screen of the system console is blanked in preparation for use by the software being deadstarted in PP0. (Note that the program used is the one displayed on the screen and does not necessarily have to be the same as one of the permanently stored special purpose programs.)

Command L

Command L (followed by **Enter**) is used to initiate a long deadstart sequence. In this sequence, the following events occur:

- A deadstart master clear is issued to the PPs and channels, and all error status bits are cleared.
- The long deadstart program, permanently stored in the TPM memory, is loaded into logical PP0 and executed. This program performs a diagnostic test that checks out the major hardware elements required for deadstart.
- The PP register display is brought up on the right-hand side of the screen while the long deadstart program is running. (This program runs for about 15 seconds).
- Certain error status bits are monitored to determine if the hardware failed during the long deadstart. In case of failure, one of the following messages is displayed below the PP register display.
 - LDS BRANCH TEST FAILURE
 - LDS PROGRAM TRANSFER ERROR
 - STATUS SUMMARY ERROR (for IOU errors only) (Refer to the Maintenance Register Display for additional error isolation information)
- If the program runs to completion without error, then a short deadstart sequence is automatically initiated, using the program currently displayed on the screen.

Deadstart Programs

Entering command S causes the 16-word program currently displayed on the console to be loaded into locations 18 through 208 of PP0, and causes execution of this program to begin at location 1. Commands are provided to enter or modify this program. Multiple programs may be created for different uses and may be saved in a special memory. Four such programs may be stored by using the command:

SP X Store Program (0 through 3)

where X is the program number (X = 0 through 3). Once a program has been stored, it may be retrieved and displayed at a later time by using the command:

GP X Get Program (0 through 7)

where X is the program number to be retrieved and displayed.

In addition to the four programs that may be stored using the SP command, there are four more (fixed) programs that can be accessed using the GP command. These programs are numbered 4 through 7. Hence, the allowable values for parameter X are 0 through 7. (Programs 4 through 7 are intended for maintenance use.) After a GP command, the program number X is displayed on the screen for reference only. If any editing of the program is done, only the local or screen version is changed. The original version in location X is not modified because stored programs can only be changed by an SP X command. (Note that it is possible to get a program from one location, perform editing, and save it in a different location, if desired.)

The user may inspect each of the deadstart programs, one after the other, by pressing the space bar on the keyboard. If the only entry in a command line is via the space bar, the next higher numbered deadstart program is displayed. After program 7 is selected, program 0 is re-selected.

Permanent Deadstart Programs 4 Through 7

Four special purpose programs are permanently stored in the TPM microcomputer memory for use by maintenance personnel. These programs should not be executed by the operator unless the customer engineer requests them.

The programs may be retrieved and displayed by using the GP X (Get Program X) command, where X is the program number. The contents of the programs are shown in figures D-6 through D-9. Maintenance functions performed by the programs are as follows:

- Program 4: Clear Errors and Master Clear: This utility issues the master clear and clear errors functions to the IOU, memory, and the CPU.
- Program 5: Channels 00 and 01 Echo Test: This program causes PP0 to echo varying data patterns across channels 00 and 01.
- Program 6: Channels 12 and 13 Echo Test: This program causes PP0 to echo varying data patterns across channels 12 and 13.
- Program 7: Channels 15 and 17 Echo Test: This program causes PP0 to echo varying data patterns across channels 15 and 17.

MAINTENANCE OPTIONS - IOU 0	
MODEL 44 (S/N 0101) REV. 01	
XX YYYYYY-CHANGE DS PRG	PROGRAM 4
XX+YYYYYY-CHANGE DS PRG INC	01 007517
S-SHORT DS	02 007717
L-LONG DS	03 000540
H-HELP	04 007717
	05 000140
	06 007717
	07 000552
	10 007717
PPM CONF = 1	11 000560
DLY LOOP = 0	12 007717
LDS ADDR = 6000	13 000572
CLK FREQ = NORMAL	14 007717
MEM SIZE = 8K	15 000160
STAT SUM = 00	16 007717
	17 000060
	20 000300

Figure D-6. Stored Deadstart Program 4, Clear Errors and Master Clear

MAINTENANCE OPTIONS - IOU 0	
MODEL 44 (S/N 0101) REV. 01	
XX YYYYYY-CHANGE DS PRG	PROGRAM 5
XX+YYYYYY-CHANGE DS PRG INC	01 007440
S-SHORT DS	02 103721
L-LONG DS	03 000406
H-HELP	04 007200
	05 007000
	06 103321
	07 000472
	10 000300
PPM CONF = 1	11 007441
DLY LOOP = 0	12 103721
LDS ADDR = 6000	13 000466
CLK FREQ = NORMAL	14 007201
MEM SIZE = 8K	15 007001
STAT SUM = 00	16 103321
	17 000472
	20 000300

Figure D-7. Stored Deadstart Program 5, Channels 00 and 01 Echo Test

MAINTENANCE OPTIONS - IOU 0	
MODEL 44 (S/N 0101) REV. 01	
XX YYYYYY-CHANGE DS PRG	PROGRAM 6
XX+YYYYYY-CHANGE DS PRG INC	01 007452
S-SHORT DS	02 103721
L-LONG DS	03 000406
H-HELP	04 007212
	05 007012
	06 103321
	07 000472
	10 000300
PPM CONF = 1	11 007453
DLY LOOP = 0	12 103721
LDS ADDR = 6000	13 000466
CLK FREQ = NORMAL	14 007213
MEM SIZE = 8K	15 007013
STAT SUM = 00	16 103321
	17 000472
	20 000300

Figure D-8. Stored Deadstart Program 6, Channels 12 and 13 Echo Test

MAINTENANCE OPTIONS - IOU 0	
MODEL 44 (S/N 0101) REV. 01	
XX YYYYYY-CHANGE DS PRG	PROGRAM 6
XX+YYYYYY-CHANGE DS PRG INC	01 007452
S-SHORT DS	02 103721
L-LONG DS	03 000406
H-HELP	04 007212
	05 007012
	06 103321
	07 000472
	10 000300
PPM CONF = 1	11 007453
DLY LOOP = 0	12 103721
LDS ADDR = 6000	13 000466
CLK FREQ = NORMAL	14 007213
MEM SIZE = 8K	15 007013
STAT SUM = 00	16 103321
	17 000472
	20 000300

Figure D-9. Stored Deadstart Program 7, Channels 15 and 17 Echo Test

Editing Deadstart Programs

Two commands are provided to edit a program displayed on the screen, these are:

```
XX YYYYYY (or XX.YYYYYY or XX,YYYYYY)
and
XX+YYYYYY
```

The first command is used to change a single word (XX) in the program to a new value (YYYYYY). The number YYYYYY may be any number having from one to six octal digits and in the range 0 through 177777. Leading zeros do not have to be typed for XX or YYYYYY.

The second command is used to change a block of sequential words in the program. As each new word is entered, the editor automatically increments the address value XX and clears the remainder of the line so that the value at the (incremented) address may be entered. Pressing the Return key before entering a data value causes the old value to remain unaffected and increments to the next XX. This block editing may be terminated by pressing the Erase key. Also, the sequence is automatically terminated when word number 20 has been entered.

Reconfiguration

In order to deadstart NOS/VE with the IOU, it is necessary that the first, second, and third logical PPs in barrel 0 be functional. If they are functional, then the system may be deadstarted and other (failing) PPs may be logically turned off using the CTI commands described under the Operator Intervention Display in the Disk Deadstart section of the CIP Reference manual. If, however, one of these PPs is not functional, then hardware reconfiguration should be used as described below to select a set of logical PPs from the available physical PPs such that the first, second, and third logical PPs in barrel 0 are good.

Hardware reconfiguration of PPs is accomplished by reconfiguring the PP memories. It should be noted that the IOU does not support barrel reconfiguration. Therefore, if barrel 0 is not functional it must be repaired before deadstart is possible. Troubleshooting is done with LDX or the TPM diagnostic.

PP memories within each barrel may be reconfigured by using the deadstart display and entering the command:

```
RP X
```

where X is the number of the physical PP memory which is to be used as logical PP memory 0. Note that X not only designates which PP in physical barrel 0 is to be PP0; it also designates which PP in physical barrel 1 will be PP5, which PP in barrel 2 will be PP20, and which PP in barrel 3 will be PP25. The value X, which may be 0, 1, 2, 3 or 4, is displayed on the line PPM CONF=X (see figure D-3).

For examples of the effects of reconfiguration, refer to figure D-10.

NOTE

The RP command takes effect only after a master clear has been issued. Commands that cause a master clear are S, L, DS, and SD. Certain packets also cause a master clear to be issued.

PHYSICAL PPMs IN EACH BARREL	RP=0				RP=1				RP=2				RP=3			
	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3	BAR0	BAR1	BAR2	BAR3
00	00	05	20	25	04	11	24	31	03	10	23	30	02	07	22	27
01	01	06	21	26	00	05	20	25	04	11	24	31	03	10	23	30
02	02	07	22	27	01	06	21	26	00	05	20	25	04	11	24	31
03	03	10	23	30	02	07	22	27	01	06	21	26	00	05	20	25
04	04	11	24	31	03	10	23	30	02	07	22	27	01	06	21	26

M02920

Figure D-10. Reconfiguration Example

Maintenance Features

The following paragraphs describe the various deadstart maintenance commands and displays. These commands and displays may be used for troubleshooting hardware failures or for diagnosing problems with system software. They allow inspection of the internal PP data and control information. In addition, they provide a means of establishing hardware scope loops for looking at failing hardware conditions.

To execute these commands, the user must first reach the IOU Maintenance Options Display (figure D-3). Refer to Software Interface for instructions on selecting the Maintenance Option display. The R command is used to return to the IOU Maintenance Options Display from any of the other maintenance displays described in this appendix.

The following commands are intended to be used by the customer engineer only and should not be executed by the operator:

- TB XX YYYYYY
- DE X
- LA YYYY
- SM
- SD
- DS

CF X (Clock Frequency)

This command is used to select the 20-MHz clock frequency margin condition. Parameter X may be F (2% faster), N (normal), or S (2% slower). It is initialized to normal when the system is powered up or the 1HKH module is inserted.

CH W (Channel Status Display)

This command causes channel status information to be displayed as shown in figure D-11. Possible values for the signals displayed are 0 and 1. Note that channel 16 is not implemented.

IOU 0 CHANNEL STATUS																	
	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17	
ACTIVE	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	
FULL	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	
FLAG	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	
ERROR	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	
	20	21	22	23	24	25	26	27	30	31	32	33					
ACTIVE	1	1	1	1	1	1	1	1	1	1	1	1					
FULL	0	0	0	0	0	0	0	0	0	0	0	0					
FLAG	0	0	0	0	0	0	0	0	0	0	0	0					
ERROR	0	0	0	0	0	0	0	0	0	0	0	0					

Figure D-11. Channel Status Display

CL (Clear LEDS)

This command is used to clear the fault LEDs on all IOU modules.

DC XX (Deadstart Channel)

This command causes a master clear to be issued to only the specified channel. The parameter XX must be an octal number in either the range 0 through 13 or 20 through 33.

DE X (Delay)

This command selects one of eight loop delay times for use with those commands that perform repeated deadstarts (SD, S, and L). The parameter X may have values 0 through 7, and is used to select the delay time from a fixed table. The times in the table are arranged from shortest (X = 0) to longest (X = 7) in logarithmic steps. Deadstart programs that execute quickly may use short delay times for maximum brightness of the oscilloscope trace. Alternatively, the delay time may be increased for longer programs to allow for full execution when scoping, or to allow time for the program to complete before the register display is updated when using the SD feature. New delay values may be entered at any time.

Loop time ranges:

S - 1.7 ms to 10.33 ms

L - 244 us to 8.85 ms

SD - 205 ms to 346 ms (Besides the DE value, SD times also depend on which display is currently being viewed.)

DS (Deadstart and Return-to-Deadstart Display)

This command causes a master clear to be issued and the 208 word deadstart program displayed on the screen is then loaded into the first logical PP in the deadstart barrel and executed. After allowing the program to execute for about 340 microseconds, the TPM microprocessor reverts to its deadstart display mode and reactivates the display that was present on the screen before the DS command was entered.

EM XXXXX YYYYY ZZZZZZ (Enter PP Memory Block)

The EM command is used to enter data pattern ZZZZZZ into the PP memory currently displayed starting from location XXXXX through location YYYYY. The parameters are similar to those of the EP command. This command may be used only when the PP memory display is active.

EP XXXXX YYYYYY (Enter PP Memory)

This command may be used when the PP memory display is active to enter data YYYYYY into location XXXXX of the PP memory currently displayed on the screen. The command may also be used in the format:

EP+XXXXX YYYYYY

This format automatically increments the address XXXXX after each entry to facilitate entering sequential blocks of data. The use of the Return key and no new data will merely increment to the next PP memory address. Sequential data entry using this second format is terminated by pressing the Delete key. The parameter XXXXX may be any octal number in the range 0 through 17777 when PP memory is in 8K mode or 0 through 7777 in 4K mode. The parameter YYYYYY may be any octal number in the range 0 through 177777. These commands may be used to perform octal patches on test programs, or to enter troubleshooting routines that are longer than 16 words and, therefore, do not fit in a normal deadstart program. In the latter case, the program entered using this command should be placed beyond word 21 (because the deadstart sequence over-writes words 0 through 21) and the deadstart program should contain a jump to the beginning of the test program.

ER XX Y ZZ (Enter Register)

This command may be used to modify the contents of the IOU maintenance registers whenever the Maintenance Register Display is active. The parameters are as follows:

XX = Register number (as described under command MR - Maintenance Register Display)

Y = Byte number (0 through 7)

ZZ = Hexadecimal data to be entered (0 through FF).

FI XX (Force Idle)

This command forces a PP idle. The parameter XX (the number of the logical PP to be idled) may be any octal number in either the range of 0 through 11 or 20 through 31. All idled PPs are reactivated by a short (S) or a long (L) deadstart.

The FI XX command may be useful in debugging software that ties up a system element (such as memory, a channel, etc.) In such a case, the IOU Maintenance Options Display should be activated, the failing PP idled, and the PP registers inspected. Note that when the IOU Maintenance Options Display is activated on the system console, both ports, as well as channel 17, become unavailable. This could result in a PP hang, so this procedure should only be used during time dedicated to software testing.

H (HELP Display)

The command H (followed by **Enter**) calls up the Help display (refer to figures D-4 and D-5). This display provides a list of commands that may be used to change deadstart programs or invoke maintenance displays. The Help display is removed by entering any command that brings up another display.

I (IOU Initialization)

This command returns the IOU to its power-up state. It causes the TPM microprocessor to perform the following operations in the order shown:

1. Disarm scope mode.
2. Set the IOU clock frequency to normal.
3. Idle all PPs.
4. Clear all PP memories in 8K mode.
5. Master clear the assembly/disassembly unit (ADU).
6. Clear fault status register errors.
7. Clear the operating system bounds register.
8. Clear the module LEDs.
9. Issue a 1-microsecond master clear.
10. Idle the first logical PP in the deadstart barrel.
11. Bring up the IOU Maintenance Options Display.

The message IOU INITIALIZATION IN PROGRESS appears on the screen while the PP memories are being cleared.

LA YYYY (Long Deadstart Address)

This command and its usage is normally restricted to factory use only. The address at which a long deadstart (LDS) begins may be set to the value YYYY through use of this command. The parameter YYYY may be any octal number in the range 0 through 7776, with 6000 being the setting for a normal LDS. Values other than 6000 may be desirable when the first portion of the LDS program runs successfully, and the hardware problem being investigated causes a failure beyond the point where a scope loop would be short enough to be feasible. In these cases, the LA command may be used to set YYYY to an address just before the point of failure, resulting in a usable scope loop. Workable starting addresses may be determined using the LDS program listing.

Loop time may be adjusted using the DE command. Note the following:

- Whenever the DE command is used, care should be taken to always return YYYY to the normal value of 6000.
- The YYYY parameter is automatically reset to 6000 at IOU power-up time.
- Addresses less than 5400 are not part of the LDS program and are executed using the pre-deadstart contents of PP0 memory.
- LDS causes PP0 addresses of 5400 and above to be overwritten with the LDS program that is stored in the TPM read-only memory.

MC (Master Clear)

This command master clears the assembly/disassembly unit (ADU) and also clears any IOU errors.

MP XX YY (Move PP Memory into Another PP Memory)

This command is used to copy the entire contents of PP memory XX to PP memory YY. If PP memory is in 4K mode, only the lower 4K of memory is transferred.

MR (Maintenance Register Display)

⚠ WARNING

This display is potentially destructive to a running system because it makes use of the maintenance access control (MAC) circuits and will conflict with any use of these circuits by a PP using channel 17. Therefore, this display should only be used when the system is hung or otherwise idled.

The MR command causes the contents of the IOU maintenance registers to be displayed on the right-hand side of the screen as shown in figures D-12 through D-14. The display consists of 8 or 16 lines, and each line consists of the register number (in hexadecimal) followed by 16 hexadecimal digits grouped in pairs (bytes) for ease of reading. (Refer to appendix B for definitions of the codes.) A description of maintenance registers 10 through A0 as shown in figure D-12 is as follows.

Register Number	Description
10	Element ID
12	Options Installed Register
18	Fault Status Mask Register
21	Operating System Bounds Register
30	Environment Control Register
40	Status Register
80	Fault Status 1 Register
81	Fault Status 2 Register
A0	Test Mode Register

MAINTENANCE OPTIONS - IOU 0											
MODEL 44 (S/N 0101) REV. 01											
XX YYYYYY-CHANGE DS PRG	PROGRAM 1	IOU MAINT REG									
XX+YYYYYY-CHANGE DS PRG INC	01 000000	10	00	00	00	00	02	44	01	01	
S-SHORT DS	02 000000	12	00	00	0F	FF	AF	FF	8F	06	
L-LONG DS	03 000000	18	00	00	00	00	00	00	00	00	
H-HELP	04 000000	21	00	00	00	00	00	00	00	00	
	05 007704	30	00	00	00	00	80	00	04	00	
	06 000301	40	00	00	00	00	00	1B	57	00	
	07 007404	80	00	00	00	00	00	00	00	00	
	10 007104	81	00	00	00	00	00	00	00	00	
PPM CONF = 0	11 007301	A0	00	00	00	00	00	00	00	00	
DLY LOOP = 0	12 000000										
LDS ADDR = 6000	13 000000										
CLK FREQ = NORMAL	14 000000										
MEM SIZE = 8K	15 000000										
STAT SUM = 00	16 000000										
	17 000000										
	20 000000										

Figure D-12. Maintenance Registers 10 through A0

Pressing the + key while the preceding registers are being displayed causes a list of the next group of registers to be displayed. This second list contains registers B0 through B9 as shown in figure D-13. A description of the register contents is as follows.

Register Number	Description
B0	Channel 0 Status Register
B1	Channel 1 Status Register
B2	Channel 2 Status Register
B3	Channel 3 Status Register
B4	Channel 4 Status Register
B5	Channel 5 Status Register
B6	Channel 6 Status Register
B7	Channel 7 Status Register
B8	Channel 10 Status Register
B9	Channel 11 Status Register

MAINTENANCE OPTIONS - IOU 0											
MODEL 44 (S/N 0101) REV. 01											
XX YYYYYY-CHANGE DS PRG	PROGRAM 1	IOU MAINT REG									
XX+YYYYYY-CHANGE DS PRG INC	01 000000	B0	00	00	00	00	00	00	00	00	00
S-SHORT DS	02 000000	B1	00	00	00	00	00	08	00	00	00
L-LONG DS	03 000000	B2	00	00	00	00	22	08	00	00	00
H-HELP	04 000000	B3	00	00	00	00	22	08	00	00	00
	05 007704	B4	00	00	00	00	22	08	00	00	00
	06 000301	B5	00	00	00	00	22	08	00	00	00
	07 007404	B6	00	00	00	00	22	08	00	00	00
	10 007104	B7	00	00	00	00	22	08	00	00	00
PPM CONF = 0	11 007301	B8	00	00	00	00	22	08	00	00	00
DLY LOOP = 0	12 000000	B9	00	00	00	00	22	08	00	00	00
LDS ADDR = 6000	13 000000										
CLK FREQ = NORMAL	14 000000										
MEM SIZE = 8K	15 000000										
STAT SUM = 00	16 000000										
	17 000000										
	20 000000										

Figure D-13. Maintenance Registers B0 through B9

Pressing the + key while the B registers are being displayed causes a third list of registers to be displayed. This third display contains registers C0 through C9 as shown in figure D-14. The register contents are described as follows:

Register Number	Description
C0	Channel 20 Status Register
C1	Channel 21 Status Register
C2	Channel 22 Status Register
C3	Channel 23 Status Register
C4	Channel 24 Status Register
C5	Channel 25 Status Register
C6	Channel 26 Status Register
C7	Channel 27 Status Register
C8	Channel 30 Status Register
C9	Channel 31 Status Register

MAINTENANCE OPTIONS - IOU 0											
MODEL 44 (S/N 0101) REV. 01											
XX YYYYYY-CHANGE DS PRG				PROGRAM 1				IOU MAINT REG			
XX+YYYYYY-CHANGE DS PRG INC				01 000000				C0	00	00	00
S-SHORT DS				02 000000				C1	00	00	00
L-LONG DS				03 000000				C2	00	00	00
H-HELP				04 000000				C3	00	00	00
				05 007704				C4	00	00	00
				06 000301				C5	00	00	00
				07 007404				C6	00	00	00
				10 007104				C7	00	00	00
PPM CONF = 0				11 007301				C8	00	00	00
DLY LOOP = 0				12 000000				C9	00	00	00
LDS ADDR = 6000				13 000000							
CLK FREQ = NORMAL				14 000000							
MEM SIZE = 8K				15 000000							
STAT SUM = 00				16 000000							
				17 000000							
				20 000000							

Figure D-14. Maintenance Registers C0 through C9

PM XX YYYYY (PP Memory)**NOTE**

This command causes the PP containing the memory to be displayed to be forced idle. Therefore, it may not be used to observe memory during program execution unless the SD command is used to deadstart repetively.

The PM command causes 1008 words of PP memory XX to be displayed on the screen, starting at address YYYYY (see figure D-15). Sequential locations are listed from left to right on each line. The start address of each line is listed to the left of that line for reference. The addresses consist of 5 octal digits and the data consists of 6 octal digits. The parameter XX selects the logical PP memory to be displayed, and may be any octal number in either the range 0 through 11 or 20 through 31. The parameter YYYYY may be any octal number in the range 0 through 17777 (0 through 7777 if memory is in 4K mode). Note that if a long deadstart sequence (LDS) was previously interrupted (or hung) without going to completion, then LDS mode will remain set in the PPs. When displaying memory for PP0 in this case, addresses greater than or equal to 6000 will contain the LDS program.

When this display is active, pressing the + or - key (no **Enter**) increments or decrements the PP memory starting address by 1008.

If the memory display for a PP of a non-existent barrel is requested, the message BARREL NOT INSTALLED is displayed.

IOU 0 NIO PP XX										SIZE = 8K									
00000	000000	000000	000062	000040	000000	000122	000043	000006											
00010	000000	010400	001200	004400	000000	011024	001312	001516											
00020	000000	000007	010433	000000	000000	001400	000000	000020											
00030	000020	000000	000304	000000	000000	000006	001744	000000											
00040	000000	006717	010570	001002	030060	030060	030061	000000											
00050	006715	000010	000002	000061	000037	000000	000003	000006											
00060	007000	000006	001400	000024	000000	000034	000007	000006											
00070	000571	001420	105400	017763	000026	000001	000000	000000											

Figure D-15. PP Memory Display

PR X (PP Register)

This command causes the PP registers, P, A, Q and K, of a physical barrel to be displayed on the right-hand side of the screen (see figure D-16). The physical barrel number is indicated above the display and the logical PP numbers within the barrel are listed in the left column of the display. PPs are numbered in octal. The contents of the P, A, Q, and K registers are displayed as octal digits.

When the PR display is active, the + and - key provide a convenient means of selecting the physical barrel to be displayed. Pressing the + key causes the current barrel to be replaced by the next higher numbered physical barrel. If the - key is pressed, the next lower numbered physical barrel replaces the current barrel.

If the registers for a non-existent barrel are requested, the message BARREL NOT INSTALLED is displayed.

MAINTENANCE OPTIONS - IOU 0				
MODEL 44 (S/N 0101) REV. 01				
XX YYYYYY-CHANGE DS PRG	PROGRAM 1	+ = ADU BUSY	BARREL = 0	
XX + YYYYYY-CHANGE DS PRG INC	01 000000	* = PP IDLE	EX BUSY = 0	
S-SHORT DS	02 000000			
L-LONG DS	03 000000	PP P A Q K		
H-HELP	04 000000	00 007712 000010 000017 007300		
	05 007704	01 177777 020000 000001 007100		
	06 000301	*02 000156 020000 000016 107700		
	07 007404	*03 000156 020000 000016 107700		
	10 007104	*04 000156 020000 000016 107700		
PPN CONF = 0	11 007301			
DLY LOOP = 0	12 000000			
LDS ADDR = 6000	13 000000			
CLK FREQ = NORMAL	14 000000			
MEM SIZE = 8K	15 000000			
STAT SUM = 00	16 000000			
	17 000000			
	20 000000			

Figure D-16. PP Register Display

R (Return to Maintenance Options Display)

The R command provides the user with a convenient means of returning to the Maintenance Option Display when desired. This command can also be used to terminate execution of the SD command.

RT (Release Terminals)

The RT command causes the TPM microprocessor to release its control of the system console. This allows the software running in the PPs control of the console and allows port 0 and port 1 to again respond to functions on channel 15. In addition, it causes the TPM to release its control of channel 17 and the maintenance access control (MAC) circuits.

SD (Short Deadstart Display Loop)

The SD command repeatedly performs short deadstart sequences, with a time between deadstarts corresponding to the delay loop setting (see DE X command). Between sequences, it updates the display currently in use. Changes may be made to the deadstart program while the display loop is running by using the command XX YYYYYY. Alternatively, the command TB XX YYYYYY may be used to repeatedly toggle selected bits in the deadstart program. These features allow the person troubleshooting the machine to "try out" various test operands and observe the effect of these operands on the hardware by looking at the current display. Thus, it is easy to identify "stuck-at-one" and "stuck-at-zero" hardware faults. In addition, while the SD command is running, new displays can be selected. Note, however, that the SM and SS commands may not be used with SD.

The following actions terminate the execution of the SD command:

- Executing the R command (the recommended termination method).
- Executing any of the commands S, L, RT, QUIT, H, D, DT, *T, or *R.

SM (Scope Mode)

The purpose of the SM scope mode command is to allow the use of an oscilloscope in troubleshooting the hardware involved in various deadstart display commands. The SM command prepares the TPM microprocessor to enter a tight loop on the next command, which may be any of the following:

- S The short deadstart program is executed repeatedly in its entirety. The TB (toggle bit) and the DE (delay) features may be used.

- L The long deadstart (LDS) program is executed repeatedly starting at the address specified by LDS ADDR=XXXX. The LA command may be used to alter this address from the initialized value of 6000, but care must be taken when choosing a different address to ensure that a valid entry point is selected. In contrast to using the short deadstart command, typing L following an SM command causes the LDS program to be loaded into PP memory only once. In the case of the S command, the short deadstart program is loaded into PP memory each time the program is executed. The DE (delay) feature may also be used.

- RP Repeatedly loads the physical PP number declared to be logical PP 0 into the hardware reconfiguration register.

- PR Repeatedly reads the P, A, Q and K registers for the first logical PP in the selected barrel.

- PM Repeatedly reads eight words of PP memory beginning at address YYYYYY of PP XX.

- EP Repeatedly writes data YYYYYYY into address XXXXX of the PP memory being displayed at the time the scope loop was entered.

- MR Repeatedly reads PP maintenance register 12₁₆ (only).

- ER Repeatedly reads and writes 8 bytes of data into byte Y of maintenance register XX₁₆. The read and write data is identical except for byte Y.

- CH Repeatedly reads the 28 status bytes containing the channel flags.

- FI Repeatedly issues an idle to PP XX.

- CF Repeatedly writes and reads the clock frequency register.

- CL Repeatedly clears the IOU LEDs.

- DC Repeatedly deadstarts channel XX.

- DS Repeatedly loads the short deadstart program and issues a master clear.

- MC Repeatedly master clears the ADU and clears IOU errors.

- SS Repeatedly reads the status summary register.

During scope mode operation, the console display is not refreshed and no further commands are accepted. Typing Ctrl-G followed by Ctrl-R is the only way to exit scope mode.

TB XX YYYYYY (Toggle Bit)

This command is used to automatically toggle selected bits in the deadstart program. Parameter YYYYYY is a string of 1 through 6 octal digits and is used as a mask to select the bits to be toggled; binary 1's in this parameter cause corresponding bits to be toggled in word XX.

The TB command is intended to be used in conjunction with the SD command or with the S command in scope mode. The selected bits are toggled during each repetition of a loop. Once this feature is selected, it may be deactivated only by typing **Ctrl-G** followed by **Ctrl-R**. Toggle time may be adjusted using the DE command.

XM XXX (Extended PP Memory On/Off)

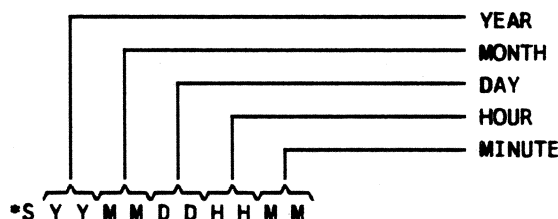
This command is used to select between 4K (normal) and 8K (extended) PP memory modes. ON selects 8K mode, OFF selects 4K mode. Executing either a short deadstart or a long deadstart resets the mode to normal.

***R (Power-On Reset)**

This command resets the TPM deadstart parameters without the need to cycle system power after the battery has failed. After executing an *R, the IOU Maintenance Options Display appears with the message RE-ENTER DS PROGRAMS.

***SYMMDDHHMM (Set Time)**

This command is used to set the calendar/clock provided the Calendar/Clock Display shown in figure D-17 is active. The clock should be set using a consecutive 24 hour time period (military time) per the following.



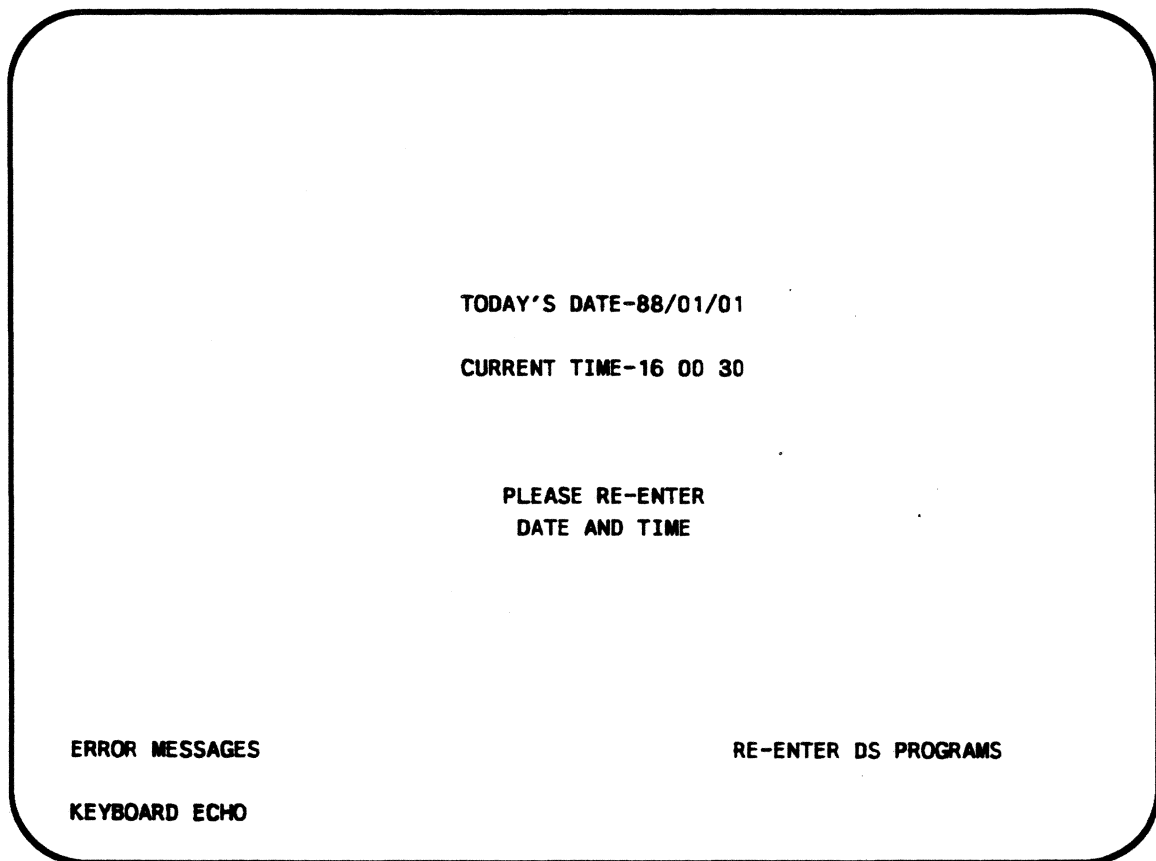


Figure D-17. Calendar/Clock Display

*T (Display Time)

This command causes the Calendar/Clock Display (figure D-17) to appear. If the calendar/clock needs to be set, the message PLEASE RE-ENTER DATE AND TIME appears.

Miscellaneous Keyboard Entries

The following keyboard entries are used to perform various command functions as indicated.

Enter	Terminates all commands except +, -, and (space bar).
Backspace	Deletes the last character entered and removes the keyboard error message if present.
Esc or Delete	Deletes the complete keyboard entry line and removes the keyboard error message if present.

Battery or RAM Failure

The TPM contains a lithium battery that maintains deadstart programs 0 through 3 and the reconfiguration status, and allows the calendar/clock to continue running with line power removed. A fresh battery will support these functions for at least 4000 hours.

If line power (50/60 Hz) is removed long enough to deplete the battery charge, or if the 1HKH module is removed from the machine, the loss of data is sensed and the following action is taken when power is re-applied:

- Deadstart programs 0 through 3 are erased and replaced with a 000300 in word 1 along with zeros in all remaining words.
- Reconfiguration and other parameters are set to default values.
- The time-of-day is erased, and a status bit is set for software to indicate a loss of time data. The Years entry is set to 88.
- When Ctrl-G, then Ctrl-R is pressed, the Maintenance Options Display is brought up instead of the Console Main Menu. The following messages are also displayed:

```
BATTERY FAILURE
RE-ENTER DS PROGRAMS
```

These messages are removed when the first entry is typed into the deadstart program on the screen.

When a TPM RAM failure is detected, the same actions are taken except that the message displayed is:

```
RE-ENTER DS PROGRAMS
```

Operator's Console Interface Diagnostic

The IOU provides a scope-loop feature for troubleshooting suspected failures in the system console. To enable the Operator's Console Interface Diagnostic, the ground plug at backpanel locations B23-A031/C031 must be removed. This causes the TPM microprocessor to repeatedly read the keyboard of the system console and echo back the last character read to the screen.

To run the Operator's Terminal Interface Diagnostic on port 0, a ground plug must be installed on the IOU backpanel at location B23-B005/D005. To run the diagnostic on port 1, a ground plug must be installed on only B23-B004/D004. If both, or neither, backpanel locations have ground plugs installed, the diagnostic will run on port 0.

Note that the baud rate of the port must be set to 4800 or higher when running this diagnostic. The default baud rate at power-up time is 19200, but it may be changed by the system console during the **Ctrl-G** sequence with the TPM.

If the interface is operating correctly, the TPM continues to paint the screen with line after line of the character typed at the keyboard. It continues to do so until the diagnostic is disabled by re-installing the ground plugs at locations B23-A031/C031, B23-B004/D004, and B23-B005/D005. Once these ground plugs have been installed, the TPM will again respond to the **Ctrl-G**, **Ctrl-R** sequence.

Two-Port Mux Internal Diagnostic (D) Tests

The internal diagnostic tests are a feature of the TPM microprocessor firmware. These tests provide a quick check of the IOU deadstart-related hardware. These tests also include scope loops to aid in troubleshooting the problems the tests uncover.

The internal diagnostic tests may be executed with either the D or DT X Deadstart Display commands. The parameter X corresponds to a test number and can be any number from 0 through 7. Command D causes the tests to execute one after the other beginning with test 0. Command DT X causes execution to begin at test X.

Either command, D or DT X, causes the Diagnostic Display as shown in figure D-18 to appear on the screen. If the test finishes without errors, the message OK appears on the screen opposite the test name. The message FAULT appears if an error is detected.

If an error is detected, the Diagnostic Display is replaced by an error message identifying the test, the failing data and the IOU modules that could be responsible for the error. After the error message has appeared, the SM (scope mode) command can be used to enable the failing test's scope loop. Pressing the - key during scope mode, causes the TPM microprocessor to begin executing the loop.

If no scope loop is desired after an error, pressing the - key without first entering the SM command causes the same test to begin executing with the next test data pattern. A + entry skips the rest of the current test and execute the following ones.

All tests, with the exceptions of 0 and 1, destroy the previous contents of the maintenance registers, the P, A, K, and Q PP registers and the first logical PP in the deadstart barrel. Table D-1 describes the internal diagnostic tests.

Table D-1. Internal Diagnostic Tests

Number	Test	Description
0	TPM RAM	Writes and reads the TPM RAM at addresses 5000 - 53FF ₈ . If no error stop occurs, the original content of the test location is preserved. The test pattern is 0 - FF ₁₆ increment by 1.
1	MAC Echo	Tests the MAC maintenance channel interface by echoing back the test pattern 0 - FF ₁₆ increment by 1.
2	OS Bounds Register	Tests the MAC interface by writing and reading byte 6 of this register. The test pattern is 0 - FF ₁₆ increment by 1.
3	BRL 0 PP Register	Initializes the P register to 7777 ₈ , the A register to 010000 ₈ , and the K register to 007100 ₈ . The Q register channel number corresponds to the PP number.
4	FS Mask Register	Tests the MAC interface by writing and reading byte 6 of this register. The test pattern is 0 - FF ₁₆ increment by 1.

(Continued)

Table D-1. Internal Diagnostic Tests (Continued)

Number	Test	Description
5	PPM 0 Test Part 1 (Data)	Writes and reads the 4K PP0 memory locations. The test pattern is 0 - 7777 ₈ increment by 401 ₈ .
6	PPM 0 Test Part 2 (Adrs)	Writes one location and checks that it has not written elsewhere. The test pattern is 125252 ₈ constant write to 0 - 4000 ₈ increment by left circular shift.

MAINTENANCE OPTIONS - IOU 0			
MODEL 44 (S/N 0101) REV. 01			
XX YYYYYY-CHANGE DS PRG	PROGRAM 1		
XX+YYYYYY-CHANGE DS PRG INC	01 000000		
S-SHORT DS	02 000000		
L-LONG DS	03 000000	DIAGNOSTICS	
H-HELP	04 000000		
	05 007704		
	06 000301	0)TPM RAM TEST.....OK	
	07 007404	1)MAC ECHO TEST.....OK	
	10 007104	2)OS BOUNDS REGISTER TEST...OK	
PPM CONF = 0	11 007301	3)BRL 0 PP REGISTER TEST....OK	
DLY LOOP = 0	12 000000	4)FS MASK REGISTER TEST.....OK	
LDS ADDR = 6000	13 000000	5)PPM 0 TEST PART 1(DATA)...RUNNING	
CLK FREQ = NORMAL	14 000000	6)PPM 0 TEST PART 2(ADDR)...	
MEM SIZE = 8K	15 000000	7)4K/8K MEM SELECT TEST.....	
STAT SUM = 00	16 000000		
	17 000000		
	20 000000		

Figure D-18. Internal Diagnostic Test Display

Deadstart Display Command Quick Reference Table

Table D-2 contains a listing of the various deadstart display commands that are available for use.

Table D-2. Quick Reference Table

Command	Description
CF X ¹	Enter clock frequency X = F (fast), N (normal), or S (slow) (The default = normal)
CH ¹	PP Channel Status Display
CL ¹	Clear IOU error LEDs
DC XX ¹	Deadstart channel (XX = 0 - 13 or 20 - 33)
D	Run the complete set of TPM internal diagnostics
DE X ¹	Enter the loop delay value 0 - 7 (default = 0)
DS ¹	Issue a deadstart master clear, execute the short deadstart program, momentarily release channel 17, then return to the current display
DT X	Run the TPM internal diagnostics starting at test X
EM XXXXX YYYYY ZZZZZ ¹	Enter data pattern ZZZZZ into PP memory starting address XXXXX to ending address YYYYY (if PP Memory Display is up)
EP XXXXX YYYYYY ¹	Enter data YYYYYY into PP memory location XXXXX (if PP memory display is up)
EP+XXXXX YYYYYY ¹	Same as above plus increment address
ER XX Y ZZ ¹	Enter data ZZ ₁₆ into byte Y of maintenance register XX ₁₆ (if the Maintenance Register Display is up)
ER+XX Y ZZ ¹	Same as above plus increment byte number
FI XX ¹	Idle PP (XX = PP number 0 - 11 or 20 - 31)
GP X ¹	Get deadstart program X (0 - 7) (default = program 0)
(space bar) ¹	Get the next deadstart program

Note:

1. This command also appears on the Help Display.

(Continued)

Table D-2. Quick Reference Table (Continued)

Command	Description
H	Help Display
I ¹	Initialize the IOU
L	Long deadstart
LA YYYY ¹	Enter octal long deadstart starting address (default = 6000)
MC ¹	Clear errors and master clear the ADU
MP XX YY ¹	Move whole PP memory XX to PP memory YY
MR ¹	PP Maintenance Register Display
PM XX YYYYYY ¹	PP Memory Display (XX = PP number 0 - 11 or 20 - 31; YYYYYY = Starting Address)
PR X ¹	PP Register Display (X = barrel 0 - 3)
R ¹	Return to the IOU Maintenance Options Display
RP X ¹	Enter PP configuration number (0 - 4) (default = 0)
RT	Release terminal
S	Short deadstart
SD ¹	Short deadstart display loop
SM	Arm the scope mode for the following commands: S, L, RP, PR, PM, EP, MR, ER, CH, FI, CF, CL, DC, D, DT, DS, XM, MC, and SS
SP X ¹	Save the screen deadstart program as PROGRAM X (0 - 3)
SS	Status summary scope loop (if scope mode is armed)
TB XX YYYYYY ¹	Toggle bits YYYYYY in word XX (initialized every deadstart to word 01, no bits toggled)
XM XXX ¹	Extend PP memory size XXX = ON (8K) or OFF (4K) (default = OFF)

Note:

1. This command also appears on the Help Display.

(Continued)

Table D-2. Quick Reference Table (Continued)

Command	Description
XX YYYYYY	Enter deadstart program data
XX+ YYYYYY	Enter deadstart program data and increment to the next deadstart program address
*R	Power-on reset
*SYMMDDHHMM	Set calendar clock time if displayed (Initialized with months, days, hours and minutes = 0, years = 88 and status bad.)
*T	Display calendar clock time
+	Increment barrels (if the PR display is on) Toggle between page 1, 2 and page 3 displays (if either the Help or MR display is on) Display the next 1008 PP memory words (if the PM display is on) Advance to the next internal diagnostic test (if a diagnostics error display is on)
-	Decrement barrels (if the PR display is on) Display the previous 1008 PP memory words (if the PM display is on) Advance to the next test pattern in current internal diagnostics test (if a diagnostics error display is on)

Note:

1. This command also appears on the Help Display.

Deadstart Programs

E

Warmstart Procedure	E-1
Setting Word 12	E-4
Setting Word 13	E-4
Selecting the Deadstart Level (NOS)	E-4
Level 0 Deadstart	E-4
Level 1 Deadstart	E-5
Level 2 Deadstart	E-5
Level 3 Deadstart	E-5
Selecting Deadstart Parameters	E-6
Selecting the CMRDECK (NOS)	E-6
Selecting the DCFIL Deck (NOS/VE)	E-6

This appendix provides information about two types of deadstart programs. Warmstart programs 0 through 3 are executed by the operator. Special purpose programs 4 through 7 are described in appendix D.

Warmstart Procedure

Warmstart is the deadstart procedure used when the controlware is loaded and functioning properly. Detailed information concerning all phases of the deadstart process is provided in the CIP Reference Manual.

The following steps summarize the procedures necessary to perform warmstart.

1. Ensure that required mass storage devices are available and that they have packs mounted.
2. Mount deadstart tape or pack.
3. Press **Ctrl-Alt-Del** keys simultaneously to reinitialize system console. Deadstart Options display will appear.
4. Hold down **Ctrl** key while pressing and releasing **F2** key.
5. Type **S** to bring up System Load Options display. If this is not desired deadstart program, type **M** to bring up Maintenance Options display. The following paragraphs describe how to retrieve or modify the deadstart program.
6. Select the correct CTI options. If deadstarting from a spun-down 834 or 836 disk unit, the CTI Initial Display will not appear until the drive has completed spinning up (about 30 seconds).
7. Continue with operating system initialization or MSL loading as described in the appropriate operating system operator's guide or MSL manuals.

The procedure to warmstart this system is similar to other computer systems except there is no deadstart panel. The warmstart programs are entered as octal numbers through the console keyboard. The deadstart device on which the deadstart tape or disk pack is mounted, its associated controller, and the channel used to access this equipment are identified by setting bits shown in the unshaded areas of figures E-1 and E-2.

Retrieve the deadstart program stored in microprocessor by entering:

GP n

n (0 through 3) is the number of the stored program. You can change individual instructions in a program, such as unit number or other parameters. These changes are not retained across deadstarts unless this new program or a modified program is stored.

You can use the space bar to cycle through the stored programs. If the correct warmstart program is not stored or a new program is to be entered and stored, the program must be entered as octal numbers.

	<u>Binary</u>				<u>Octal</u>
1	001	100	000	010	1402
2	111	011	0cc	ccc	73cc
3	000	000	001	111	0017
4	111	101	1cc	ccc	75cc
5	111	111	0cc	ccc	77cc
6	eee	ddd	ddd	ddd	eddd
7	111	100	0cc	ccc	74cc
10	111	001	0cc	ccc	71cc
11	111	011	000	001	7301
12	000	000	000	cfa	0000
13	rrr	ppp	xxx	xxx	rp [†] xx
14	000	000	000	000	0000
15	000	000	000	000	0000
16	000	000	000	000	0000
17	000	000	000	000	0000
20	111	001	001	010	7112

[†]The instructions for setting the bits represented by these parameters are given under Setting Word 13.

Figure E-1. Program Settings for Warmstart from Channel with a PP

	<u>Binary</u>				<u>Octal</u>
1	000	000	000	000	0000
2	000	000	000	000	0000
3	000	000	000	000	0000
4	111	101	1cc	ccc	75cc
5	111	111	0cc	ccc	77cc
6	eee	ddd	ddd	ddd	eddd [†]
7	111	100	0cc	ccc	74cc
10	111	001	0cc	ccc	71cc
11	111	011	000	001	7301
12	000	000	000	cfa	0000
13	rrr	ppp	xxx	xxx	rp ^{††} xx
14	000	000	000	000	7112

[†]eddd for tape; dddd for disk deadstart.

^{††}The instructions for setting the bits represented by these parameters are given under Setting Word 13.

Figure E-2. Program Settings for Warmstart from Channel without a PP

Change the warmstart program by entering:

xx yyyyyy (or xx.yyyyyy, or xx,yyyyyy)

xx is octal row number of the deadstart instruction and yyyyyy is the octal number equivalent to the actual instruction.

When you enter a six-digit instruction, the first two digits of the instruction must be zeros. Leading zeros in both the octal row number and the instruction, however, need not be entered. For example, if the row number was 03 and the instruction was 000017 you could enter

3 17

and get the same setting as entering:

03 000017.

If you want the system to automatically increment the octal row number, the entry after which the increment is to occur is:

xx+yyyyyy

The + character indicates that the system is to automatically increment the octal row number. When the automatic increment is in effect, the system displays the next location after accepting the previous entry. Only the next instruction need be entered.

To cancel the automatic incrementing, press the **Esc** key after the octal row number appears.

To store a new program or a modified program, enter:

SP n

n (0 through 3) is the number of the program to be stored. If a program is already stored at the specified number, the new program replaces it.

After entering or retrieving the desired warmstart program, enter

S

then press the **Enter** key for a short deadstart sequence, or enter

L

then press the **Enter** key for a long deadstart sequence.

If you want the microprocessor to automatically retrieve the warmstart program (stored as program number 3) and initiate a long deadstart sequence, store the warmstart program as program number 3. If you do not want this feature, store the first word of program 3 as 000300. This instruction puts the program in PP0 into a loop. No deadstart activity occurs and no displays appear on the screen.

Setting Word 12

The a field in bit 11 of deadstart program word 12 allows you to enter the model type that HIVS/MSL 15X uses to select extended deadstart testing. The f field in bit 10 determines whether or not the alternate PP is initialized when maintenance (M) is selected.

The a field specifies the EDS option. If you set this bit and enter L after entering or retrieving the warmstart program, the system loads and executes EDS. If you do not set this bit or enter S after entering or retrieving the warmstart program, the EDS does not occur. When this bit is set, parts of PP memories are destroyed.

If the f field is clear when Maintenance Options are selected from the Console Main Menu, f specifies that the alternate PP used for passing handoff data from CTI to the MSL is to be initialized. If f is set when Maintenance Options are selected, CTI does not initialize the alternate PP. The alternate PP does not access central memory regardless of the setting of bit f.

When you are coldstarting a tape or disk controller from a card reader, bit f is also used as part of the channel number of the card reader. Thus, the channel number of the card reader controls whether the EDS occurs when you entered an L after loading the warmstart program. If the channel number is an odd number, the EDS takes place. If the channel number is an even number, the EDS does not take place.

Setting Word 13

Three unique fields exist in word 13 of the deadstart program, which allow you to select the CMRDECK, the deadstart parameters, and the level of deadstart. The rrr field (bits 0 through 2) specifies the level of deadstart (not used by NOS/VE). The ppp field (bits 3 through 5) specifies the deadstart parameters. The xxx xxx field (bits 6 through 11) specifies the CMRDECK number (NOS) or DCFIELD number (NOS/VE).

Selecting the Deadstart Level (NOS)

You can select one of four levels of deadstart by setting the rrr field in word 13.

Level 0 Deadstart

A setting of 000 indicates an initial or level 0 deadstart during which the system is loaded from the deadstart file. This is not considered a recovery deadstart although permanent files, queued files, and system dayfiles are recovered automatically unless those file types are initialized by the EQPDECK entry, INITIALIZE. If queued files are recovered, they are inactive (refer to the QREC utility in the NOS 2 Analysis Handbook for more information). An attempt to recover these files is made on all levels of system deadstart. A level 0 deadstart is normally specified:

- For the first deadstart following a period in which the system was either inoperative or used for purposes other than NOS operations.
- When a system malfunction occurred and other levels of system deadstart prove ineffective.

If it is necessary to redeadstart the system (for example, due to system malfunction), it is recommended that you attempt a level 3 recovery deadstart. If you select level 0, the system is reloaded from the deadstart file. All PP contents are destroyed by the memory confidence test.

Level 1 Deadstart

A setting of 001 indicates a level 1 recovery deadstart during which the system, all jobs, and all active files are recovered from checkpoint information on mass storage. Permanent files are also recovered. You can do a level 1 deadstart only if the DSD command CHECK POINT SYSTEM is successfully executed immediately prior to deadstart. A level 1 deadstart does not work if the contents of the extended memory are destroyed. Once a level 1 recovery deadstart begins, all PP contents are destroyed by the memory confidence test.

Normally you use a level 1 recovery deadstart to allow maintenance to be performed and then to resume normal processing. It is also useful in system test situations. Never use level 1 recovery deadstart to attempt recovery from a system malfunction or to preserve queue files.

Level 2 Deadstart

A setting of 010 indicates a level 2 recovery deadstart during which all jobs and active files are recovered from checkpoint information on mass storage. No attempt is made to recover the system. Instead, the system is loaded from the deadstart file as in a level 0 deadstart. In all other respects, a level 2 recovery deadstart is identical to that described for a level 1 recovery deadstart. Once a level 2 recovery deadstart begins, all PP contents are destroyed by the memory confidence test.

Normally you use a level 2 recovery deadstart in system test situations; it is not recommended for the normal production environment.

Level 3 Deadstart

A setting of 011 indicates a level 3 recovery deadstart during which all jobs, active files, and the system, with the exception of the library directory, are recovered from central memory tables. Only PP memory confidence testing occurs during a level 3 recovery deadstart; central memory is unaffected.

Normally you perform a level 3 recovery deadstart following an equipment malfunction (for example, channel or PP hung), providing central memory and mass storage remain intact. Unless you can determine that central memory is no longer reliable, you should attempt a level 3 recovery following a malfunction. If level 3 recovery fails, you must perform a level 0 deadstart.

Attempting a level 1 or 2 recovery deadstart after a level 3 deadstart fails does not correctly recover system activity and can endanger system and permanent file integrity. You must perform a level 0 deadstart.

Selecting Deadstart Parameters

You can select deadstart parameters to control miscellaneous deadstart functions by setting the ppp field (bits 3 through 5) in word 13.

Bit	State	Description
3	0	Reserved for future use.
4	0	Reserved for future use.
5	0	For NOS, indicates that the CMRDECK or the level option display is not displayed during deadstart. For NOS/VE, indicates that no operator pause is to occur during deadstart.
5	1	For NOS, indicates that the CMRDECK is displayed during levels 0, 1, and 2 deadstart. Level 3 options are displayed on a level 3 deadstart. For NOS/VE, indicates that operator pause is to occur during deadstart.

Selecting the CMRDECK (NOS)

The CMRDECK defines the table sizes and other information to be used for system operations. Up to 64 CMRDECKs (numbered 0 through 778) can be included on the deadstart file.

You can select the CMRDECK only during a level 0 (initial) deadstart. For a level 1 or 2 (recovery) deadstart, you must use the CMRDECK selected during the most recent level 0 deadstart.

The number of the selected CMRDECK is indicated by setting the xxx xxx field (bits 6 through 11) in word 13. For example, if CMRDECK number 268 is selected, the corresponding switches on the deadstart panel are set as follows:

rrr ppp 010 110

Selecting the DCFIELD Deck (NOS/VE)

The DCFIELD deck contains some of the system core commands for NOS/VE. Up to 64 DCFIELD decks (numbered 0 through 778) can be included on the deadstart file. The number of the DCFIELD deck to be used is selected in word 13 (bits 6 through 11).

Panel Maps

F

This appendix shows the location of all logic modules. Figures F-1 and F-2 show the system console modules, figures F-3 through F-6 show the IOU modules, figure F-7 shows the CM modules, and figure F-8 shows the CP modules.

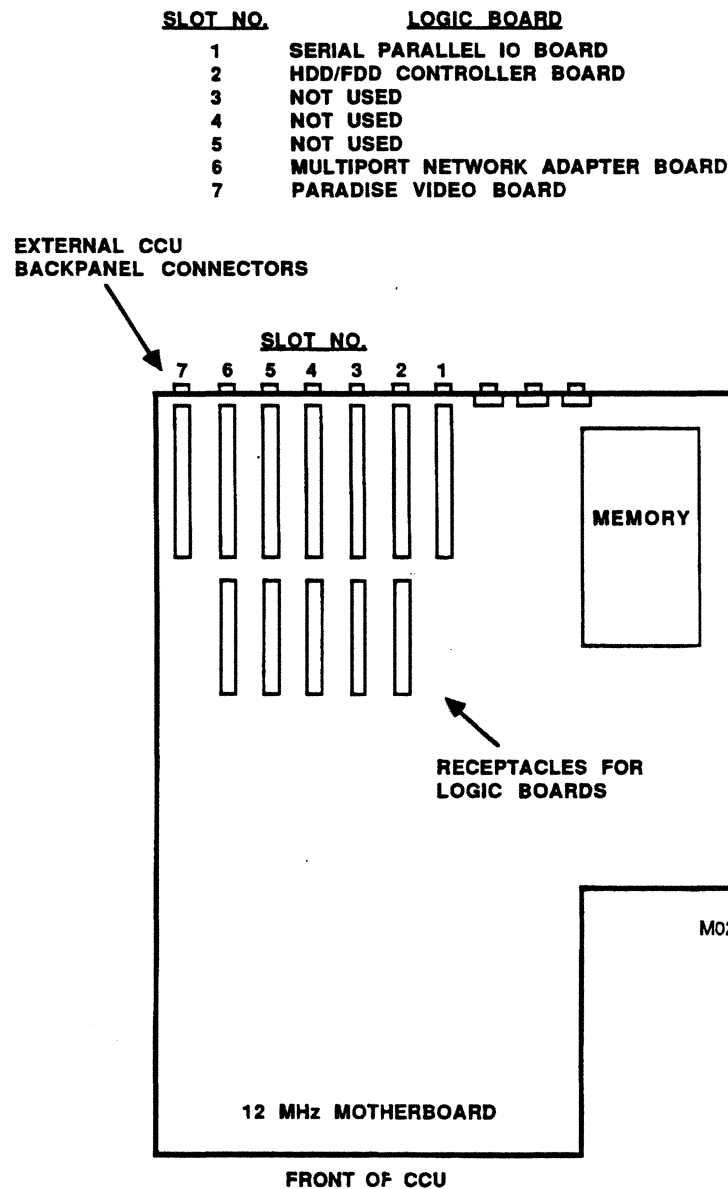


Figure F-1. System Console Panel Map for CYBER 960, Top View

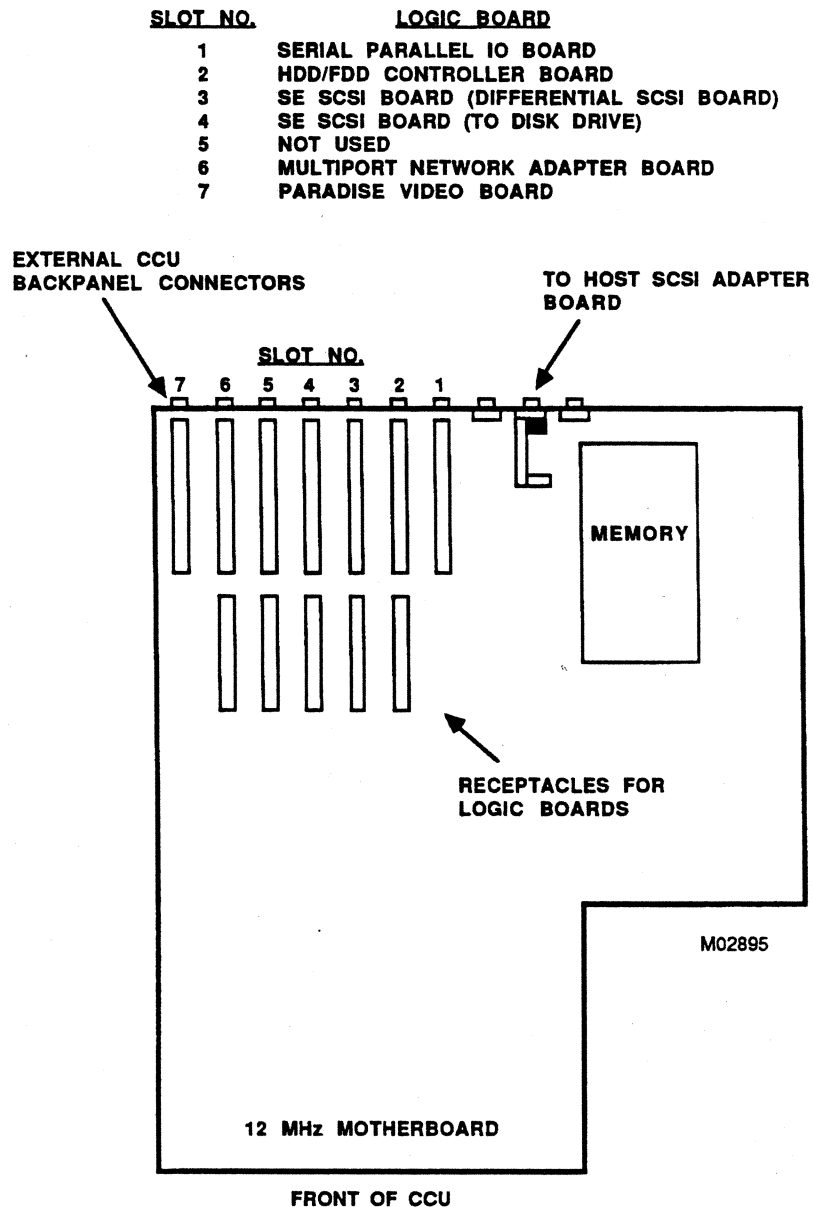
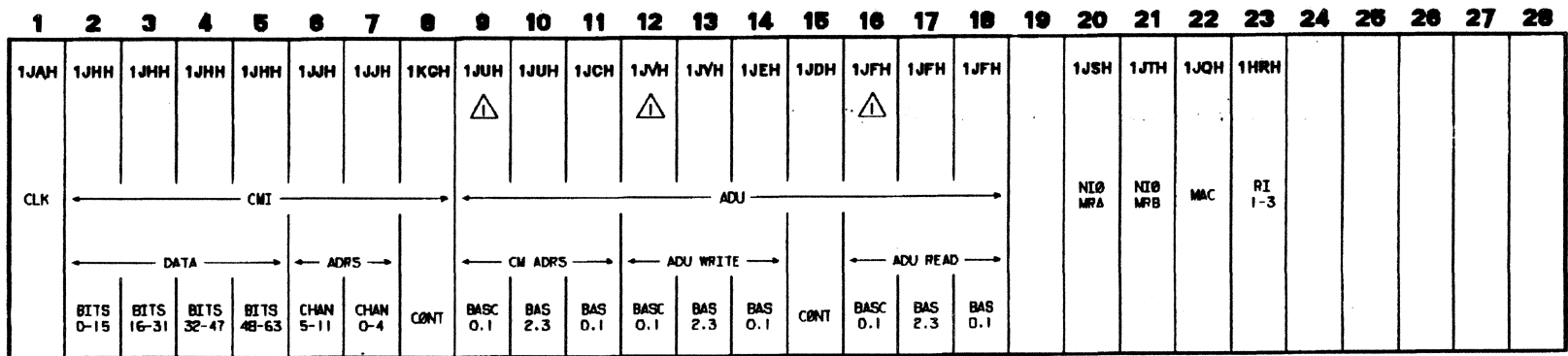


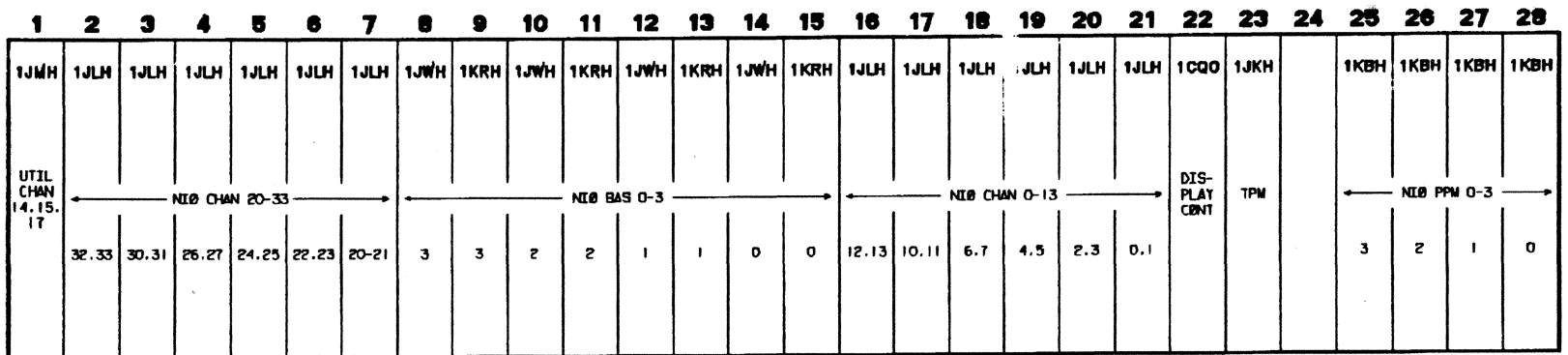
Figure F-2. System Console Panel Map for CYBER 962, Top View

Figure F-3. IOU Panel Map for CYBER 960 (NIO)

PANEL A



PANEL B



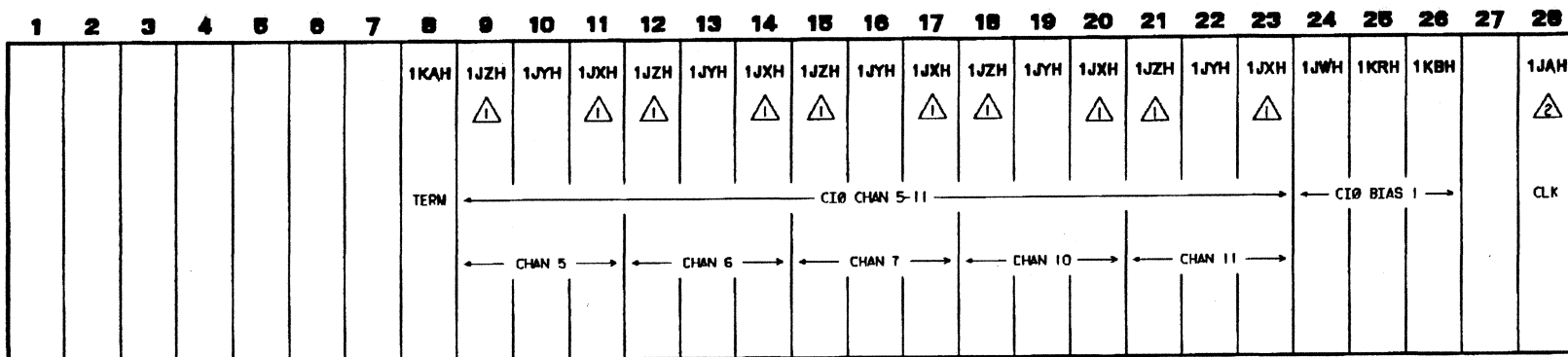
NOTE:



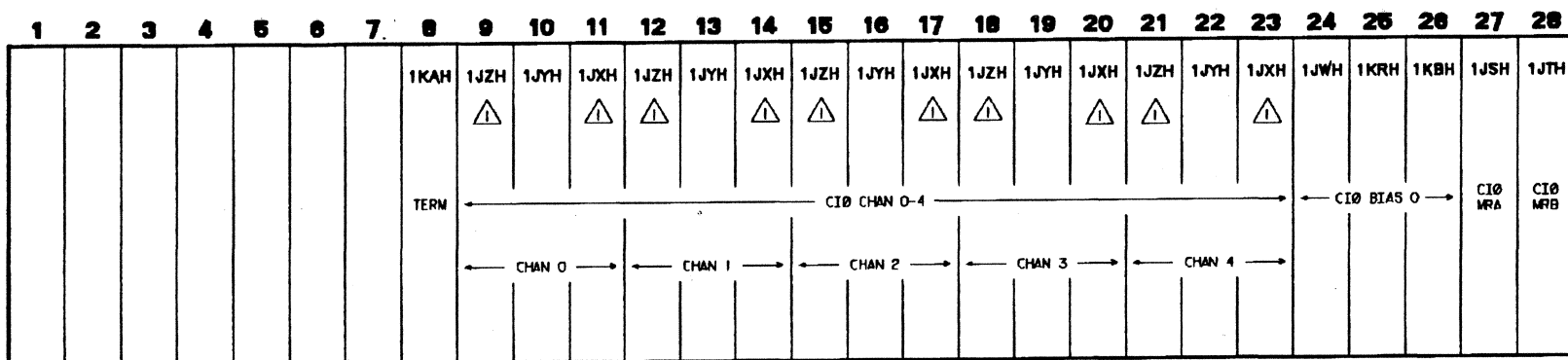
THESE 1JFH, 1JUH, AND 1JVH BOARDS ARE PART OF FIRST CONCURRENT PP INCREMENT (PANEL D).

10 100 000

SECOND CONCURRENT PP INCREMENT PANEL C



FIRST CONCURRENT PP INCREMENT PANEL D



NOTE:



1JXH AND 1JZH BOARDS ARE FOR ISI CHANNEL ADAPTER.
IF ITO DMA CHANNEL ADAPTER IS INSTALLED,
1KXH AND 1KZH BOARDS ARE AT THESE LOCATIONS.
IF IPI CHANNEL ADAPTER IS INSTALLED,
1LXH AND 1LZH BOARDS ARE AT THESE LOCATIONS.



1JAH BOARD IS PART OF FIRST CONCURRENT
PP INCREMENT (PANEL D).

Figure F-4. IOU Panel Map for CYBER 960 (CIO)

Figure F-5. IOU Panel Map for CYBER 962, Panels A and B

PANEL A

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1KAH	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1HWH	1KRH	1KBH	1HAH	1HTH	1JVH	1JFH	1HCH	1GXH	1GXH	1GXH	1GXH
TERM	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	UCODE K.C	A.P. D.R	PPM	CLK	MRB. ADU CENT	ASSY	DIS- ASSY	ADRS	R/T	R/T	R/T	R/T
← CHAN 5 →		← CHAN 6 →		← CHAN 7 →		← CHAN 10 →		← CHAN 11 →		← BAS 1 →		← ADU 0.1 →		← CHAN →													

PANEL B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1HQH	1HMH	1HLH	1KLH	1KAH	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1HWH	1KRH	1KBH	1HSH		1HKH	1HRH	1HJH	1HHH	1HHH	1HGH	1HHH	1HHH	1HJH
MAC	UTIL CHAN 14,15, 17	INT CHAN 0,1, 12,13	SCSI CHAN 32,33	TERM	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	UCODE, K.C	A.P. D.R	PPM	MRA	SPARE	TPM	RI 1-3	ADRS	DATA	DATA	CENT	DATA	DATA	ADRS
					← CHAN 2 →		← CHAN 3 →		← CHAN 4 →		← BAS 0 →							← CMI A →									

NOTE:



1JXH AND 1JZH BOARDS ARE FOR ISI CHANNEL ADAPTER.
IF ITO DMA CHANNEL ADAPTER IS INSTALLED.
1KXH AND 1KZH BOARDS ARE AT THESE LOCATIONS.
IF IPI CHANNEL ADAPTER IS INSTALLED.
1LXH AND 1LZH BOARDS ARE AT THESE LOCATIONS.

10-8 100
2000000 1

SECOND PP INCREMENT
PANEL C

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
1KAH	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1HWH	1KRH	1KBH	1HAH	1HTH	1JYH	1JFH	1HCH					
TERM	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	UCODE. K.C	A.P. O.P	PPM	CLK	MRB. ADJ CONT	ASSY	DIS- ASSY	ADRS					
← CHAN 25 →		← CHAN 26 →		← CHAN 27 →		← CHAN 30 →		← CHAN 31 →		← BAS 3 →		← ADJ 2,3 →		← SPARE →														

FIRST PP INCREMENT
PANEL D

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1KAH	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1JZH ⚠	1JYH	1JXH ⚠	1HWH	1KRH	1KBH		1HSH	1HJH	1HHH	1HHH	1HGH	1HHH	1HHH	1HJH
TERM	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	EXTI	A/D	BASI	UCODE K.C	A.P. Q.R	PPM	SPARE	MRA	ADRS	DATA	DATA	CONT	DATA	DATA	ADRS
	← CHAN 20 →			← CHAN 21 →			← CHAN 22 →			← CHAN 23 →			← CHAN 24 →			← BAS 2 →					← CMI B →						

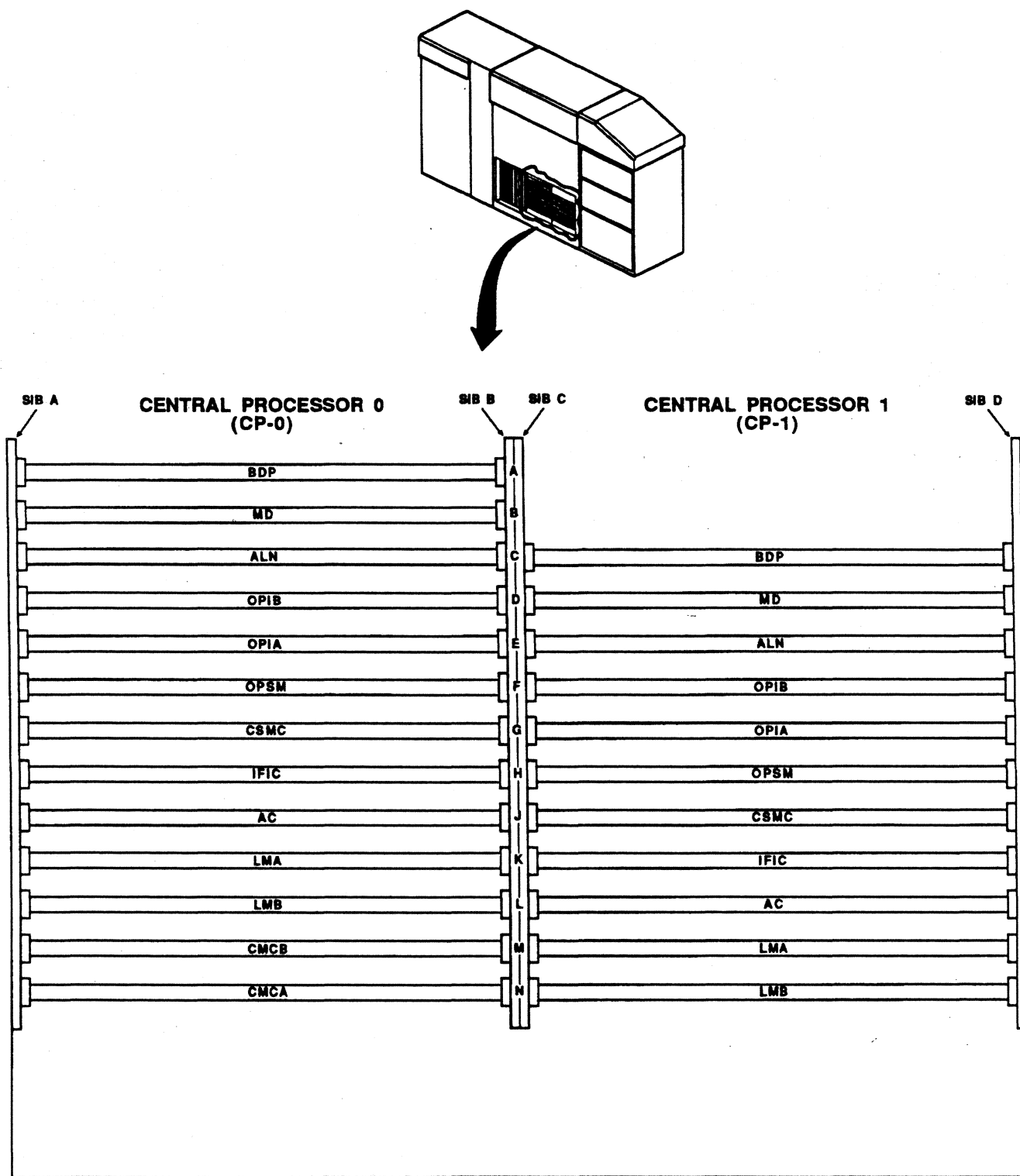
NOTE:



1JXH AND 1JZH BOARDS ARE FOR ISI CHANNEL ADAPTER.
IF ITO DMA CHANNEL ADAPTER IS INSTALLED,
1KXH AND 1KZH BOARDS ARE AT THESE LOCATIONS.
IF IPI CHANNEL ADAPTER IS INSTALLED,
1LXH AND 1LZH BOARDS ARE AT THESE LOCATIONS.

Figure F-6. IOU Panel Map for CYBER 962, Panels C and D





M02283

Figure F-8. CP Panel Map

Glossary

G

C

CE

Customer engineer.

Central Memory (CM)

The main memory of the CYBER 960/962 within the central processing unit cabinet. CM stores between 64 and 256 megabytes of data on 4 to 16 memory modules. CM hardware includes memory modules, a dedicated logic cage, a memory interface module, and voltage regulator modules.

Central Memory Control (CMC)

The logic element in the CPU that controls the movement of data between central memory (CMCA and CMCB) and the central processor. The CMC circuits reside on two logic modules located in the CP-0 logic cage, but accomplish memory control for both CP-0 and CP-1.

Central Processing Unit (CPU)

The main processing cabinet in the CYBER 960 Series mainframe, which includes the central processor (CP-0 and CP-1), central memory control, and central memory. The CPU cabinet has up to two central processors and between 64 and 256 megabytes of resident memory.

Central Processor (CP)

The functional processing logic within the CYBER 960/962 CPU. The first (or standard) central processor is referred to as CP-0. If a second central processor is provided with a system, it is referred to as CP-1. Each central processor resides in a separate logic cage and consists of eleven logic modules.

CHS

CYBER Hardware Support.

CPU

See Central Processing Unit.

CYBER 960 Series (960/962) Computer Systems

Includes CYBER 960 and CYBER 962 computer systems. The CYBER 960 Series is Control Data's state-of-the-art middle- to high-range system, flanked by the 930 departmental computer on the low end and the 990 computer on the high end of the scalar performance spectrum. A full 960 system includes the mainframe (CPU, IOU, and power unit), MG set, system console, operating software, and a complement of peripherals.

E

EEW

Express deadstart dump. //PUB

See Early Environmental Warning.

F**FCC**

Federal Communication Compliance.

FCO

Field change order.

Federal Communication Compliance (FCC)

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device (insert peripheral computing device if appropriate) pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

FRU

See Field-Replaceable Unit.

FSC

Fault symptom code.

I**Input/Output Unit (IOU)**

IOU contains the peripheral processors and channels that enable operator interaction with, and peripherals access to, the central processing unit. The IOU has either NOS and NOS/VE capability (CYBER 960) or is NOS/VE only (CYBER 962). The IOU has the interface port for the system console.

IOU

See Input/Output Unit.

L**LDS**

Literature Distribution Services.

M**MAF**

Maintenance action form.

P**Power unit**

Provides power to support the electrical systems (logic, environmental, and so on) of the CPU. (The IOU has its own power supply.) The power unit occupies a cabinet that attaches to the CPU.

Primary IOU

The IOU cabinet(s) bolted to the CPU; the IOU and, if present, the IOU non-standalone expansion.

T**TPM**

Two-port multiplexer.

Please fold on dotted line;
seal edges with tape only.

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